EE 330

Lecture 35

Cascaded Amplifiers

Differential Amplifiers

Amplifier Biasing

Other Amplifier Structures

High Frequency Performance of Amplifiers

Parasitic Capacitances in MOS Devices

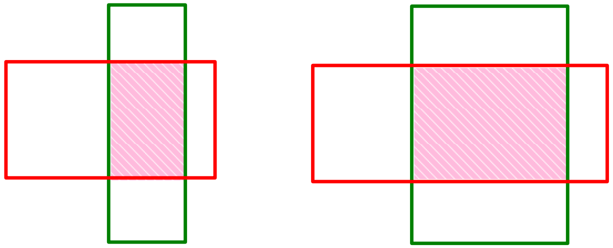
Fall 2025 Exam Schedule

Exam 1	Friday	Sept 26
Exam 2	Friday	October 24
Exam 3	Friday	Nov 21
Final Exam	Monday	Dec 15 12:00 - 2:00 PM

Review From Previous Lecture

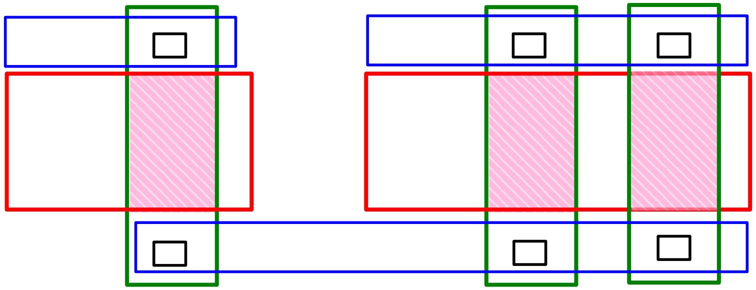
Layout of Current Mirrors

Example with M = 2



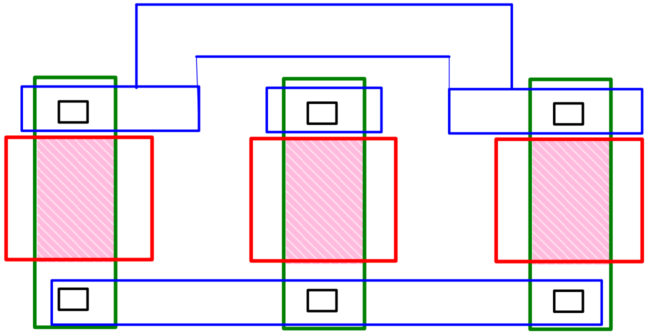
Standard layout

$$M=\left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]$$



Better Layout

$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$



Even Better Layout

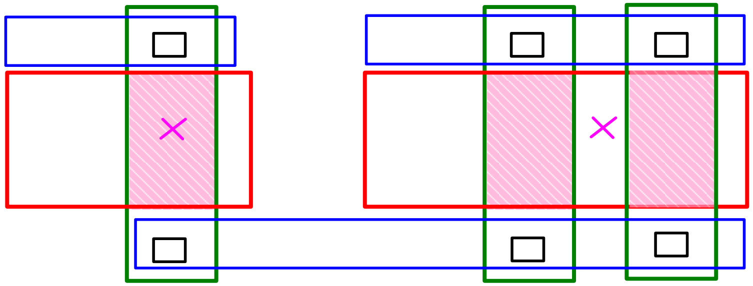
$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$

- **This is termed a common-centroid layout**
- **Linear gradient mismatch eliminated with common-centroid layout !**

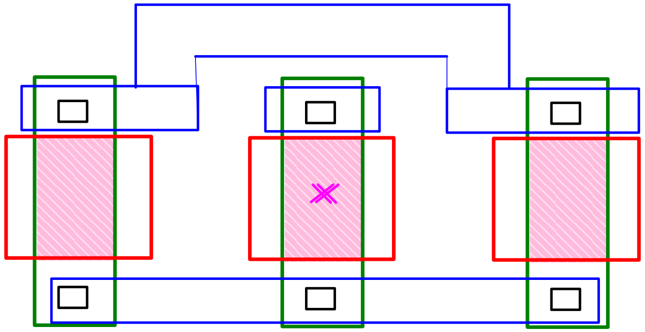
Review From Previous Lecture

Layout of Matching-Critical Circuits

Example with M = 2



Better Layout

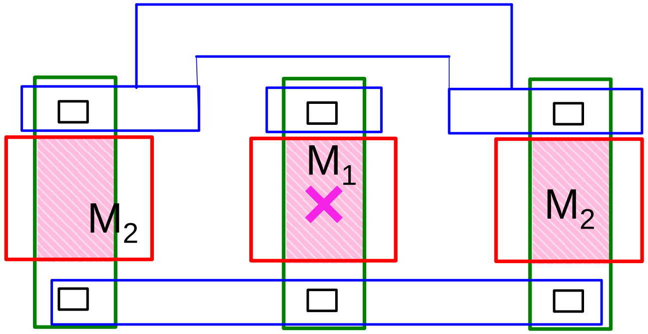


Common-centroid Layout

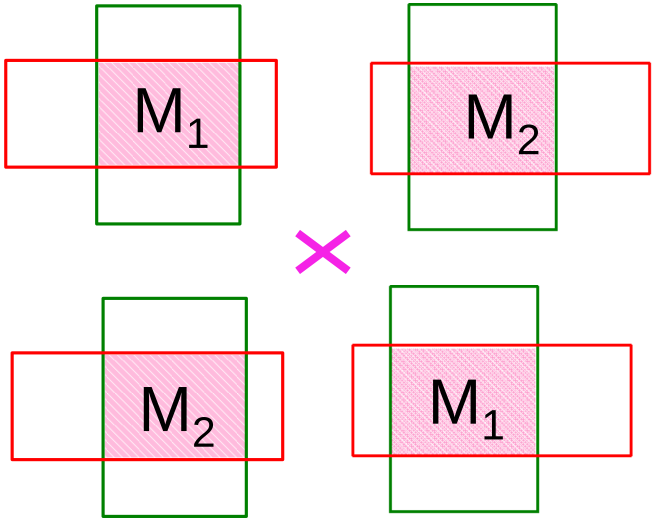
Theorem: Linear gradient mismatch eliminated with common- centroid layout !

Review From Previous Lecture

Common-Centroid Layouts



$$M=\left[\frac{2W_1}{W_1}\bullet\frac{L_1}{L_1}\right]=2$$



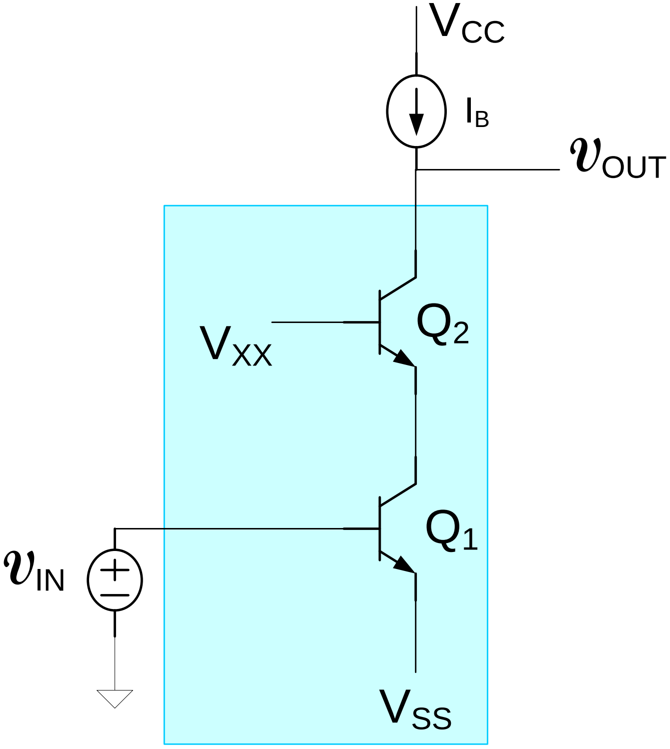
$$M=\left[\frac{2W_1}{2W_1}\bullet\frac{L_1}{L_1}\right]=1$$

- Individual transistors often decomposed into parallel multiple unary devices connected in parallel
- Common-Centroid layout approach widely used to minimize (ideally cancel) gradient effects in matching-critical circuits
- Applications extend well beyond current mirrors
- More than 2 devices can share a common centroid

Review From Previous Lecture

Cascode Configuration

Discuss



$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{02}}\beta\right] \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

$$g_{0CC} \cong \frac{g_{02}}{\beta}$$

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta = \left[\frac{2V_{AF}}{V_t}\right]\beta = [-8000]100$$

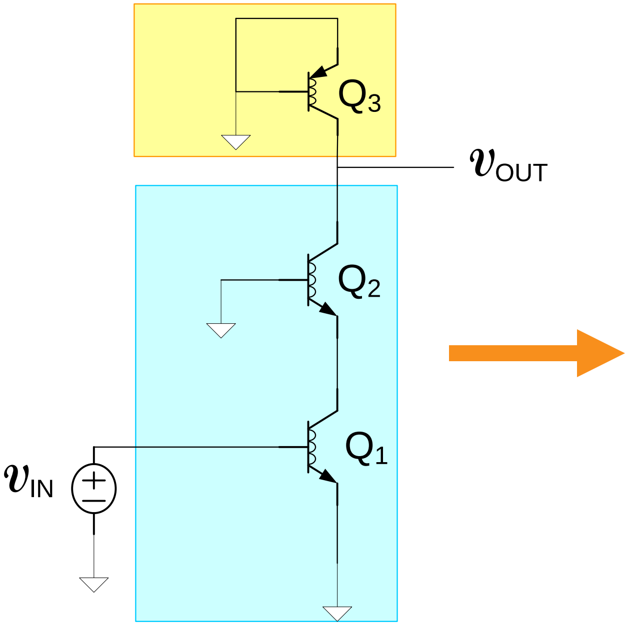
$$A_{VCC} \cong -800,000$$

This gain is very large and only requires two transistors!

What happens to the gain if a transistor-level current source is used for I_B?

Review From Previous Lecture

Cascode Configuration



$$A_V \cong A_{VCC}\left[\frac{g_{0CC}}{g_{03}}\right] \cong \frac{A_{VCC}}{\beta}$$

But recall

$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

Thus

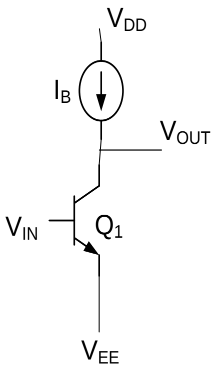
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

$$A_V \cong -\left[\frac{I_{CQ}/V_t}{I_{CQ}/V_{AF}}\right] = -\left[\frac{V_{AF}}{V_t}\right] \cong -8000$$

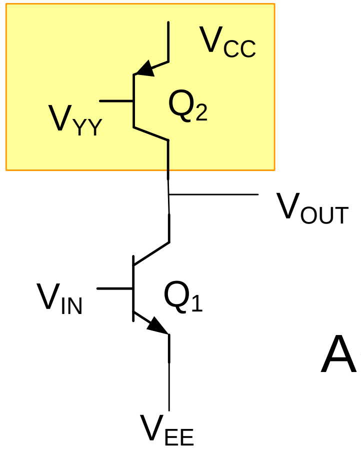
- **This is still a factor of 2 better than that of the CE amplifier with transistor current source** $\left(A_{VCE} \cong -\left[\frac{g_{m1}}{2g_{01}}\right]\right)$
- **It only requires one additional transistor**
- **But its not nearly as good as the gain the cascode circuit seemed to provide**

Review From Previous Lecture

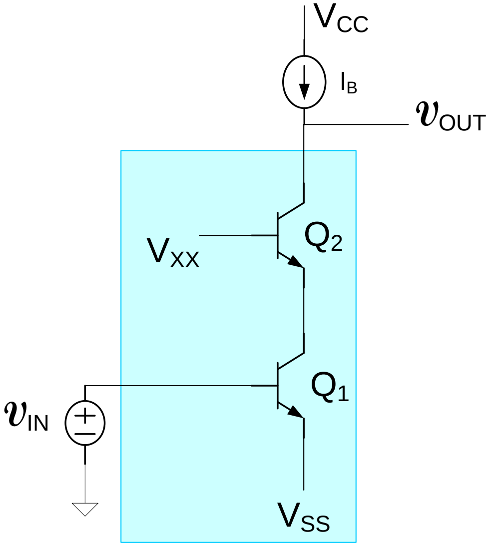
Cascode Configuration Comparisons



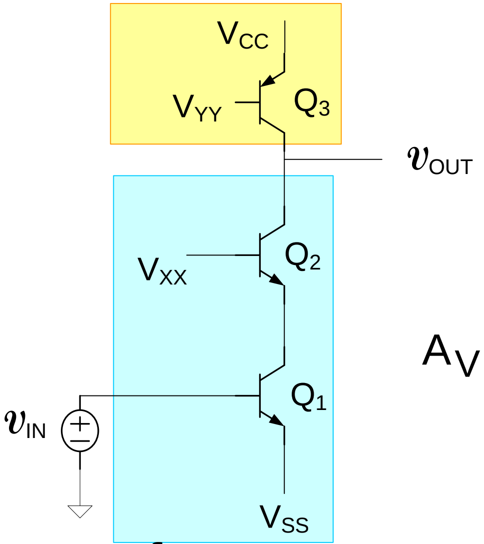
$$A_V = \frac{-g_m}{g_0}$$



$$A_V \cong \frac{-g_{m1}}{g_{01}+g_{02}} = \frac{-g_{m1}}{2g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



$$A_V \cong -\left[\frac{g_{m1}}{\frac{g_{01}}{\beta}+g_{03}}\right] \cong -\left[\frac{g_{m1}}{g_{03}}\right]$$

Gain limited by output impedance of current scource !!

Can we design a better current source?

In particular, one with a higher output impedance?

Better current sources

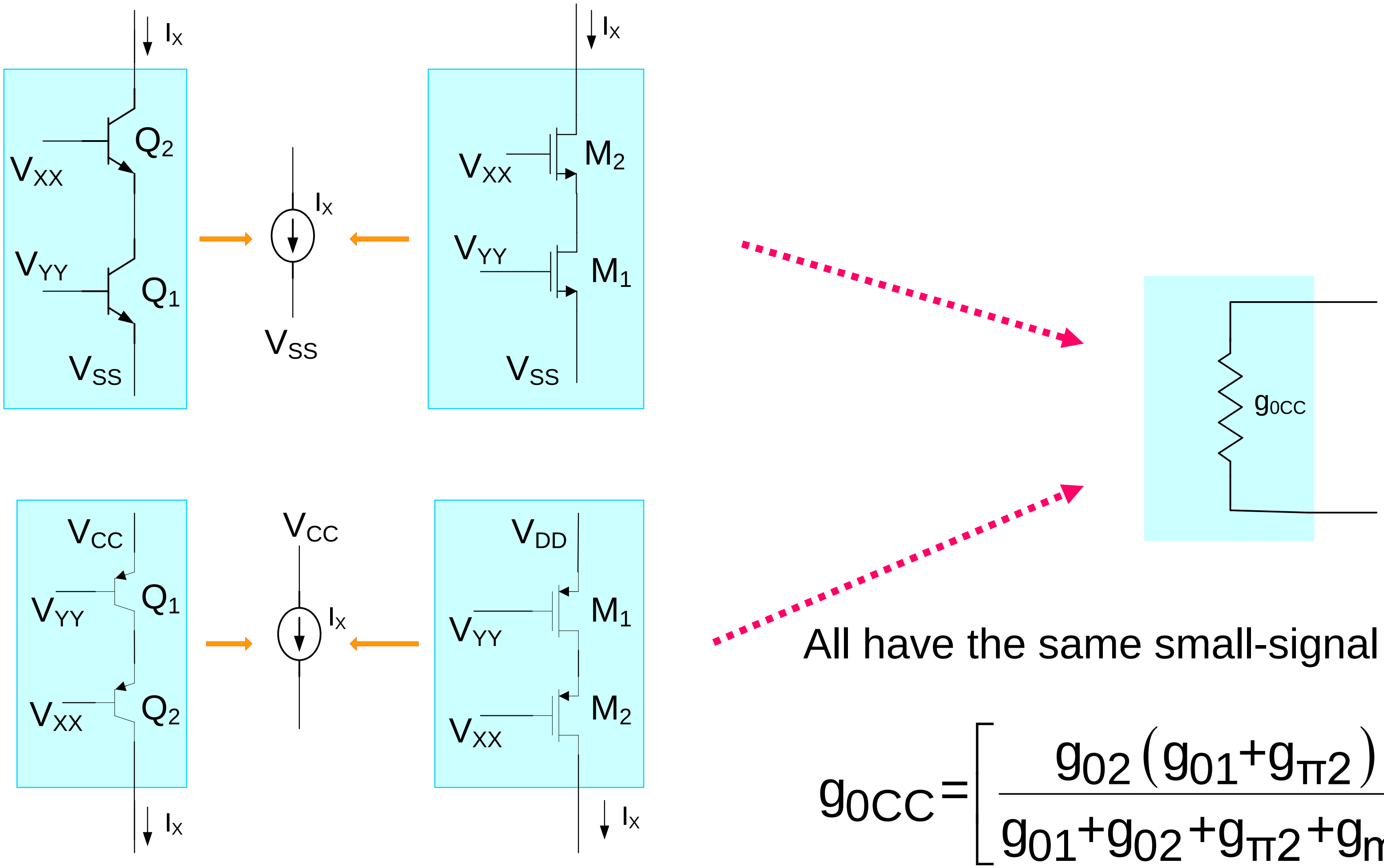
Need a higher output impedance than g_o

The output impedance of the cascode circuit itself was very large !

$$g_{0CC} \cong \frac{g_{01}}{\beta}$$

Can a current source be built with the cascode circuit ?

Cascode current sources

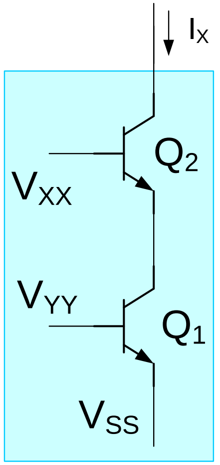


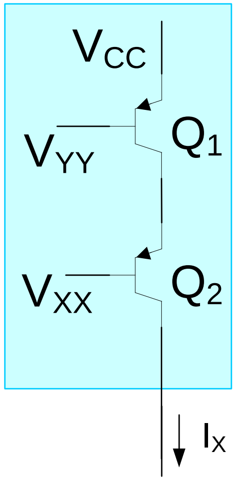
All have the same small-signal model

$$g_{0CC}=\left[\frac{g_{02}\left(g_{01}+g_{\pi2}\right)}{g_{01}+g_{02}+g_{\pi2}+g_{m2}}\right]$$

Review From Previous Lecture

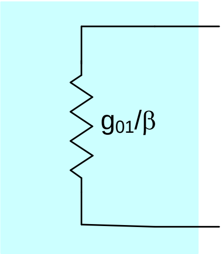
Cascode current sources





For the BJT cascode current sources

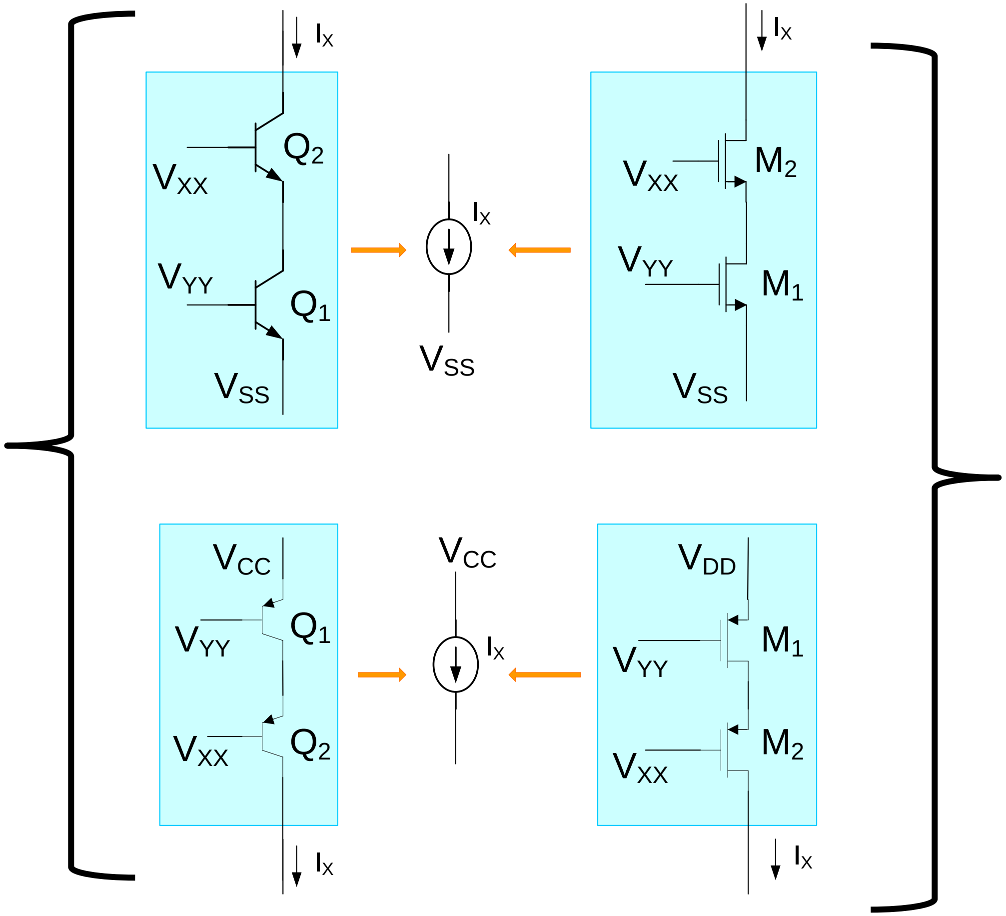
$$g_{0CC}=\left[\frac{g_{02}\left(g_{01}+g_{\pi 2}\right)}{g_{01}+g_{02}+g_{\pi 2}+g_{m2}}\right]\cong\left[\frac{g_{02}g_{\pi 2}}{g_{m2}}\right]=\frac{g_{01}}{\beta}$$



Review From Previous Lecture

Cascode current sources

$$g_{0CC} \simeq \frac{g_{01}}{\beta}$$



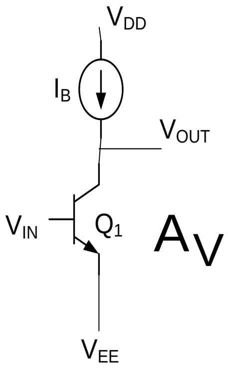
$$g_{0CC} \simeq g_{01}\frac{\lambda V_{EB}}{2}$$

- Cascode current sources have a much higher output impedance that the basic single-transistor current sources
- No increase in power dissipation (current re-use concept)
- Moderate loss in headroom

Review From Previous Lecture

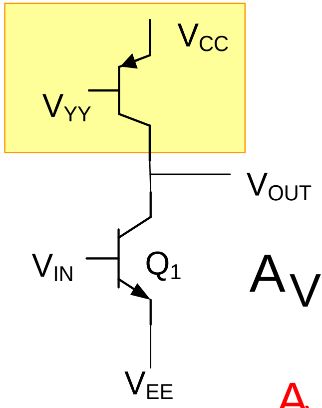
Cascode Configuration Comparisons

Discuss



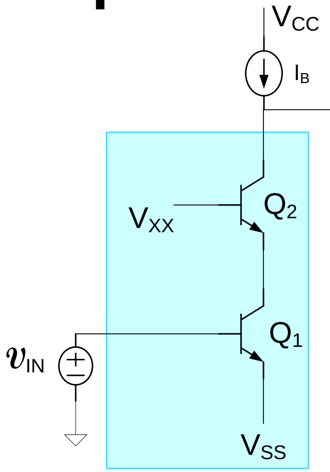
$$A_V = \frac{-g_m}{g_0}$$

A_V= -8,000



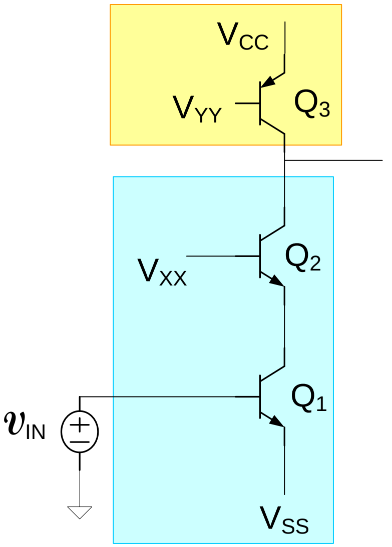
$$A_V \cong \frac{-g_{m1}}{2g_{01}}$$

A_V= -4,000



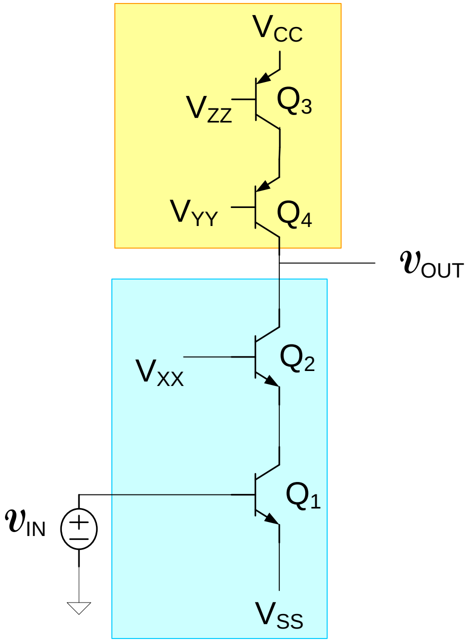
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$

A_V= -800,000



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

A_V= -8,000



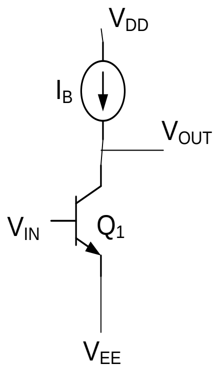
$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

A_V= -400,000

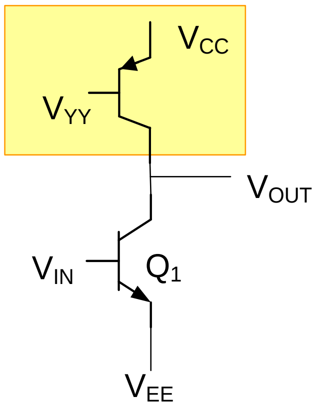
Can we use more cascoding to further increase the gain?

Review From Previous Lecture

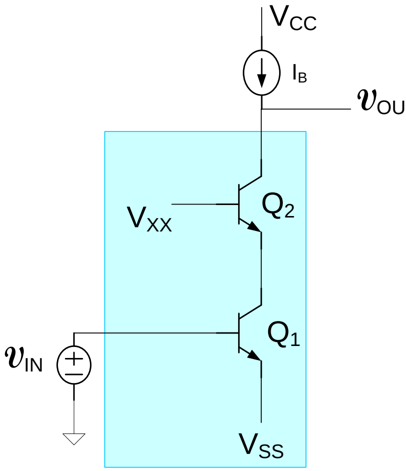
High Gain Amplifier Comparisons (BJT)



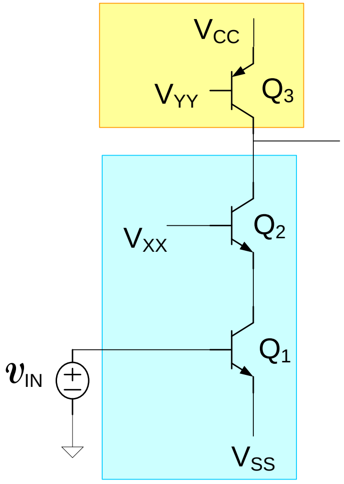
$$A_V = \frac{-g_m}{g_0}$$



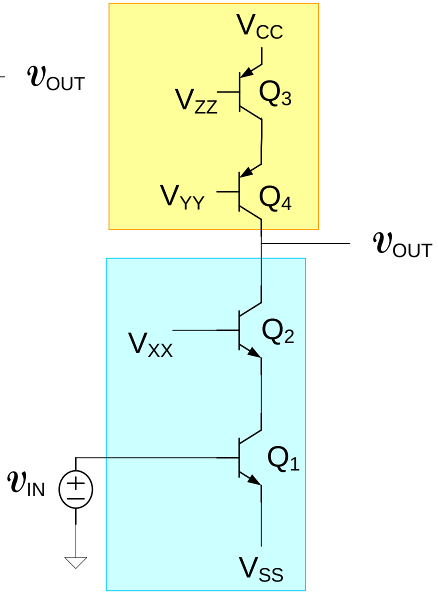
$$A_V \cong -\frac{1}{2}\frac{g_{m1}}{g_{01}}$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]\beta$$



$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$

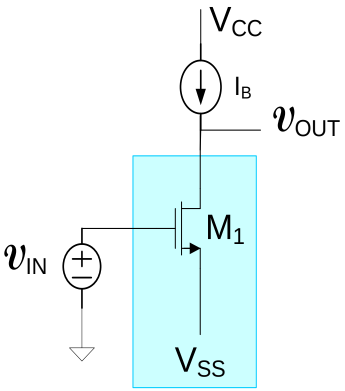


$$A_V = -\left[\frac{g_{m1}}{g_{01}}\right]\frac{\beta}{2}$$

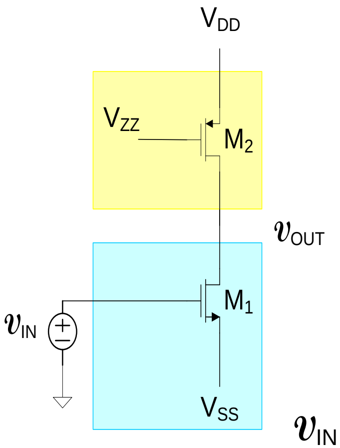
- Single-ended high-gain amplifiers inherently difficult to bias (because of the high gain)
- Biasing becomes practical when used in differential applications
- These structures are widely used but usually with differential inputs

Review From Previous Lecture

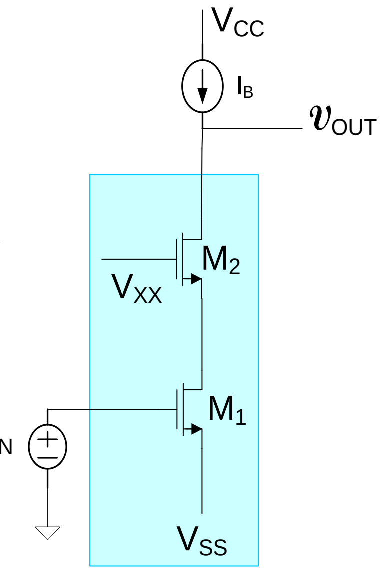
High Gain Amplifier Comparisons (n-ch MOS)



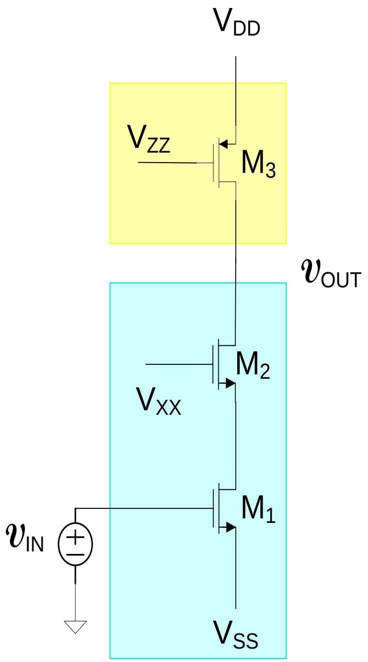
$$A_V \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



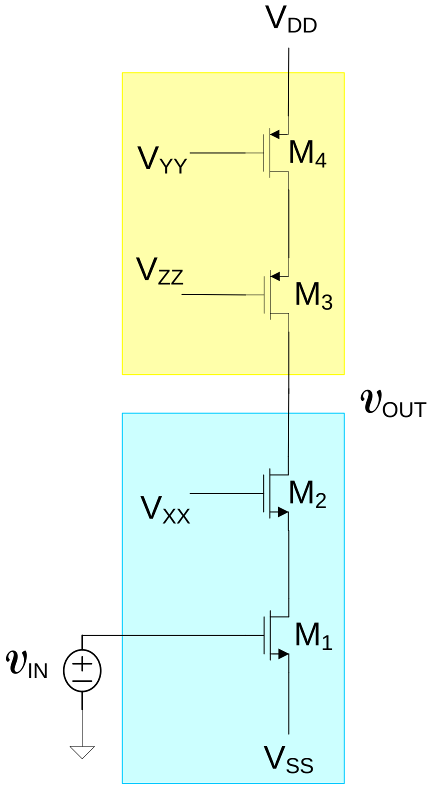
$$A_V \cong -\frac{1}{2}\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_{VCC} \cong -\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

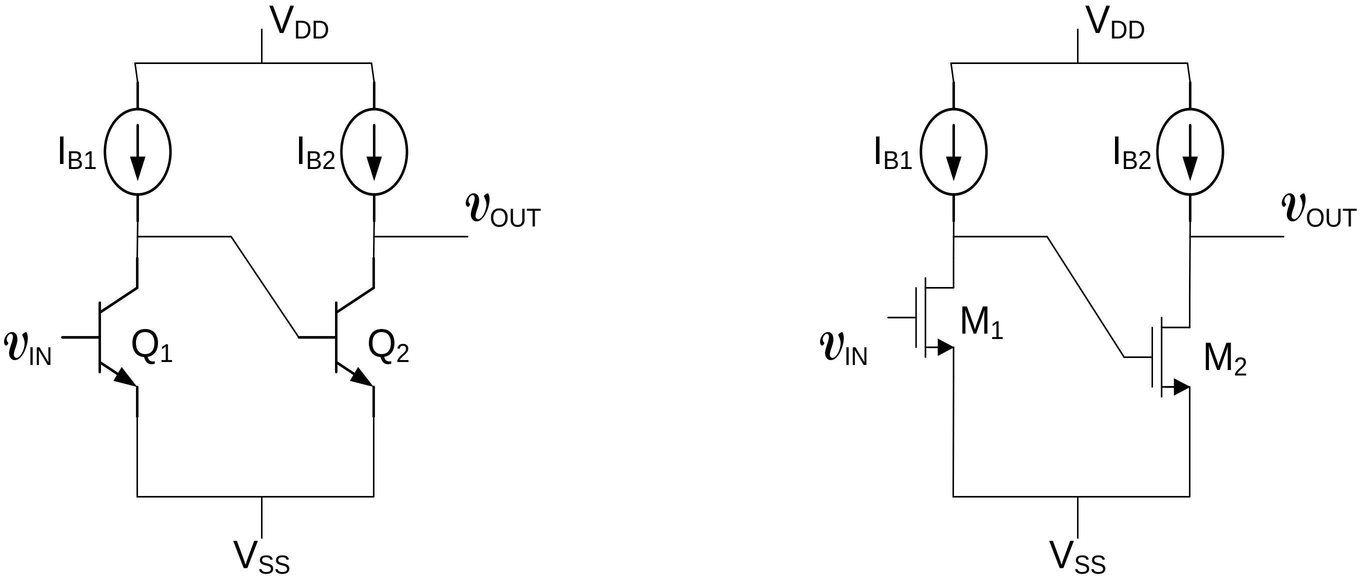


$$A_{VCC} \cong -\left[\frac{g_{m1}}{g_{01}}\right]$$



$$A_{VCC} \cong -\frac{1}{2}\left[\frac{g_{m1}g_{m2}}{g_{01}g_{02}}\right]$$

Cascade Configurations

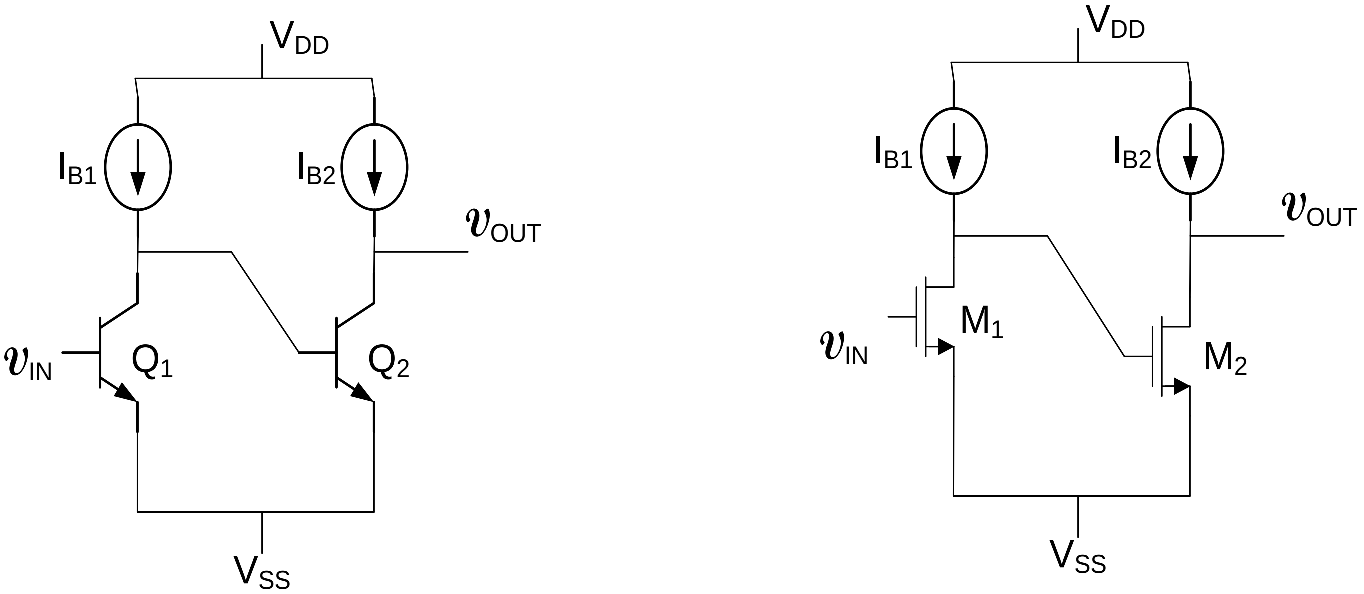


Two-stage CE:CE or CS:CS Cascade

$$A_{VCB} = ?$$

$$A_{VCM} = ?$$

Cascade Configurations



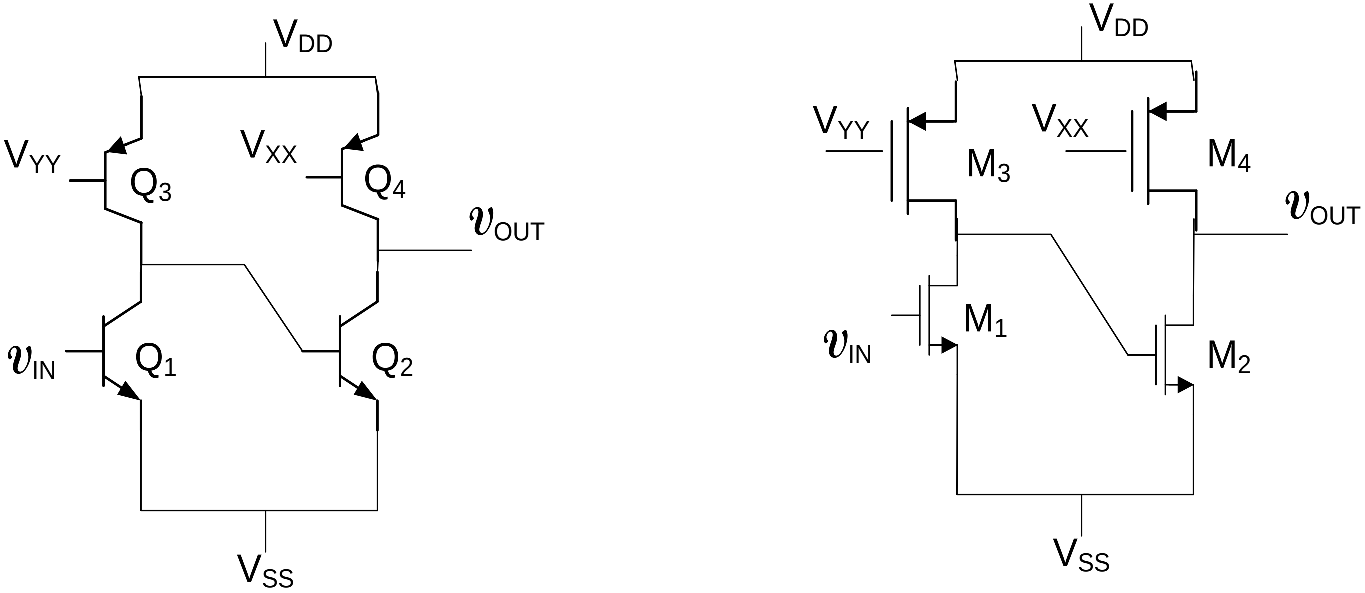
Two-stage CE:CE or CS:CS Cascade

$$A_{VCB} \cong \left[\frac{-g_{m1}}{g_{01}+g_{\pi 2}}\right]\left[\frac{-g_{m2}}{g_{02}}\right] \cong \frac{g_{m1}g_{m2}}{g_{\pi 2}g_{02}} = \beta\frac{g_{m1}}{g_{02}}$$

$$A_{VCM} = \left[\frac{-g_{m1}}{g_{01}}\right]\left[\frac{-g_{m2}}{g_{02}}\right] = \frac{g_{m1}g_{m2}}{g_{01}g_{02}}$$

- **Significant increase in gain**
- **Gain is noninverting**
- **Comparable to that obtained with the cascode but noninverting**

Cascade Configurations



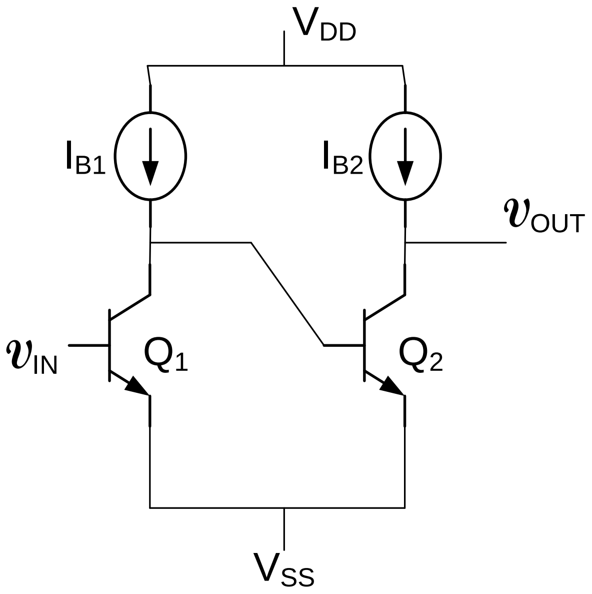
Two-stage CE:CE or CS:CS Cascade

$$A_{VCB} \cong \left[\frac{-g_{m1}}{g_{01}+g_{03}+g_{\pi 2}}\right]\left[\frac{-g_{m2}}{g_{02}+g_{04}}\right] \cong \frac{g_{m1}g_{m2}}{2g_{\pi 2}g_{02}} = \beta\frac{g_{m1}}{2g_{02}}$$

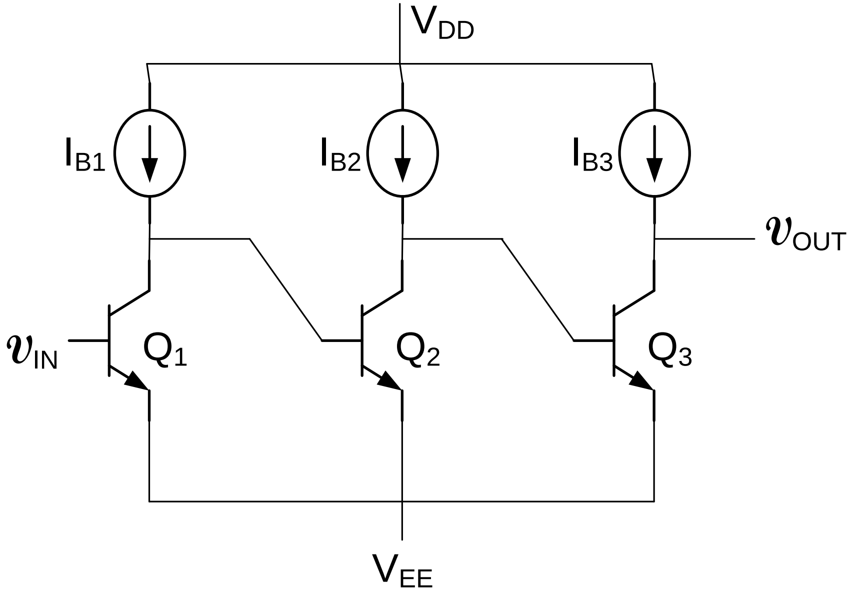
$$A_{VCM} = \left[\frac{-g_{m1}}{g_{01}+g_{03}}\right]\left[\frac{-g_{m2}}{g_{02}+g_{04}}\right] = \frac{g_{m1}g_{m2}}{4g_{01}g_{02}}$$

Note factor or 2 and 4 reduction in gain due to actual current source bias

Cascade Configurations



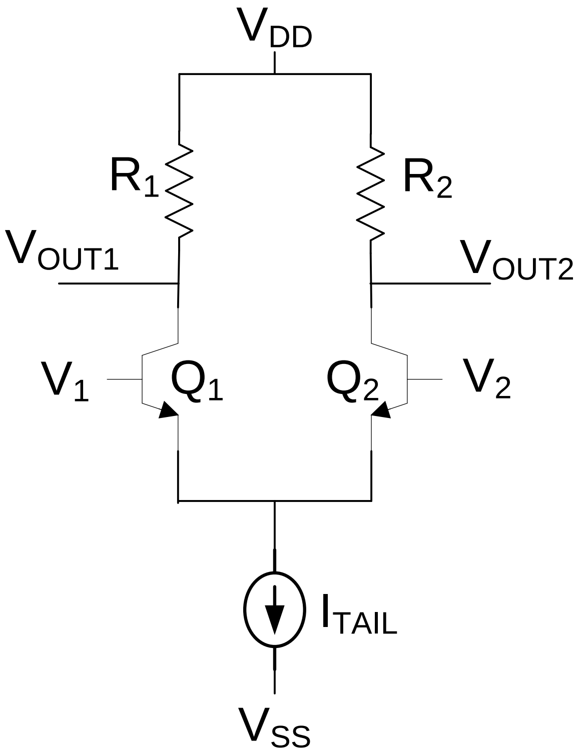
Two-stage CE Cascade



Three-stage CE Cascade

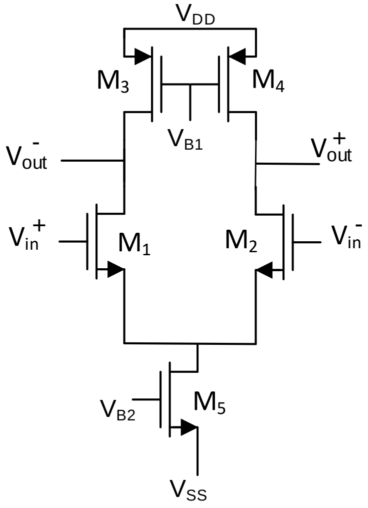
- **Large gains can be obtained by cascading**
- **Gains are multiplicative (when loading is included)**
- **Large gains used to build “Op Amps” and feedback used to control gain value**
- **Some attention is needed for biasing but it is manageable**
- **Minor variant of the two-stage cascade often used to build Op Amps**
- **Compensation of two-stage cascade needed if feedback is applied to maintain stability**
- **For many years three or more stages were seldom cascaded because of challenges in compensation to maintain stability though recently some industrial adoptions**

Differential Amplifiers

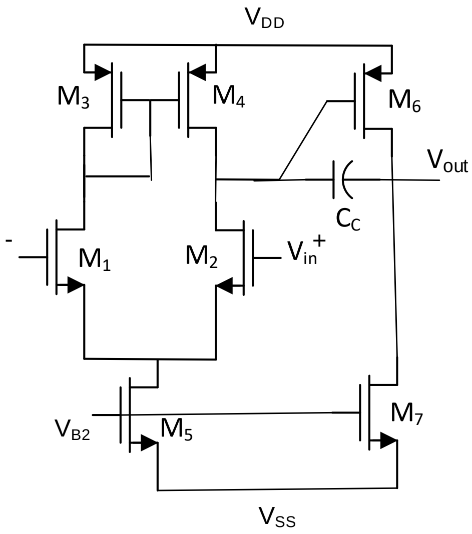


A basic operational amplifier circuit

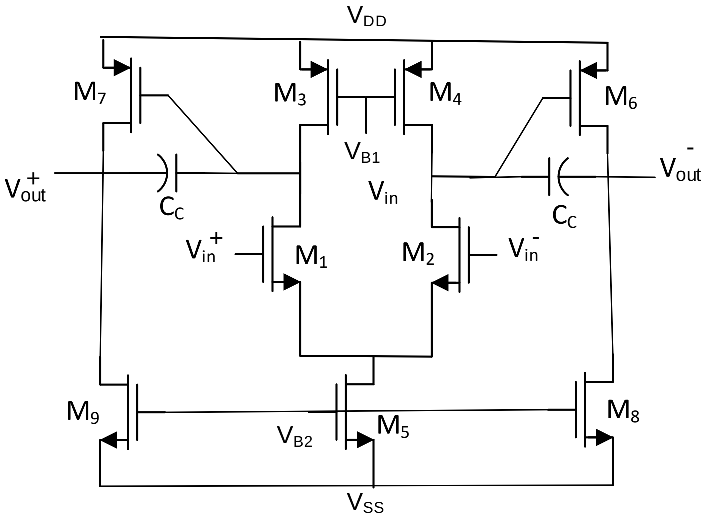
Differential Amplifiers



5T Op Amp



7T Op Amp



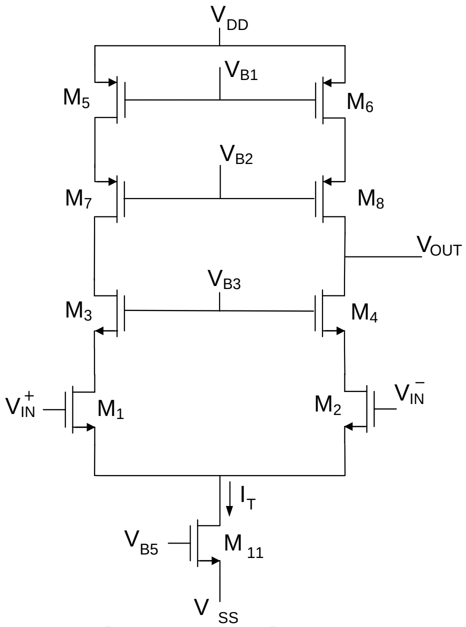
9T Op Amp

Basic MOS operational amplifier circuits

(CMFB not shown for 9T op amp)

The Cascode Amplifier

- Operational amplifiers often built with basic cascode configuration
- CMFB used to address the biasing problem
- Usually configured as a differential structure when building op amps
- Have high output impedance (but can be bufferred)
- Terms “telescopic cascode”, “folded-cascode”, and “regulated cascode” often refer to op amps based upon the cascode configuration



Telescopic Cascode Op Amp

(CMFB feedback biasing not shown)

Amplifier Biasing

Amplifier biasing is that part of the design of a circuit that establishes the desired operating point (or Q-point)

Goal is to invariably minimize the impact the biasing circuit has on the small-signal performance of a circuit

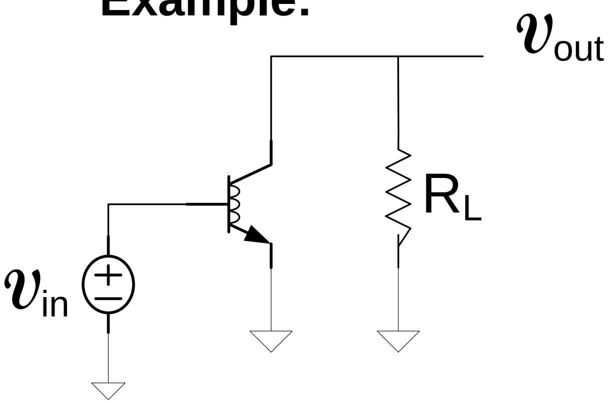
Usually at most 2 dc power supplies are available and these are often fixed in value by system requirements – this restriction is cost driven

Discrete amplifiers invariable involve adding biasing resistors and use capacitor coupling and bypassing

Integrated amplifiers often use current sources which can be used in very large numbers and are very inexpensive

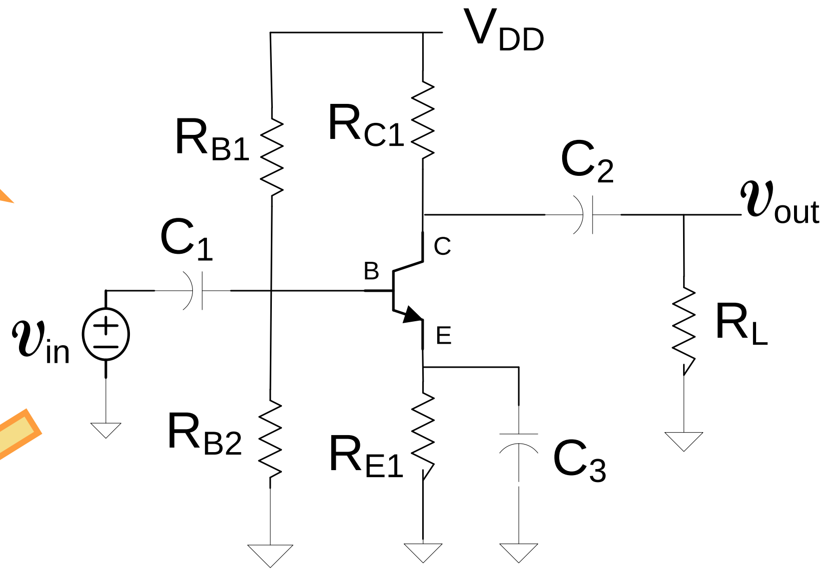
Amplifier Biasing

Example:

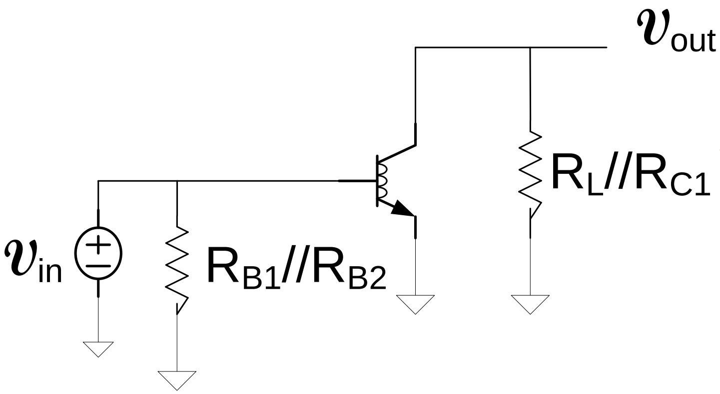


$$A_V = -g_m R_L$$

Desired small-signal circuit
Common Emitter Amplifier



Biased circuit

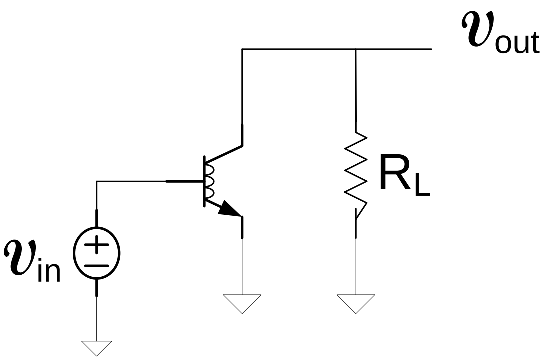


Actual small-signal circuit

$$A_V = -g_m \left(R_L // R_{C1} \right)$$

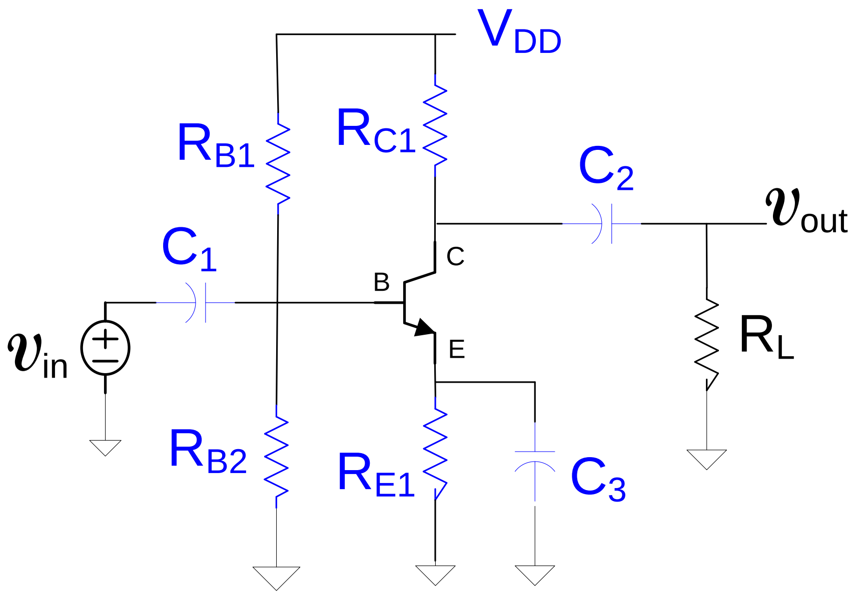
Amplifier Biasing

Example:



Desired small-signal circuit
Common Emitter Amplifier

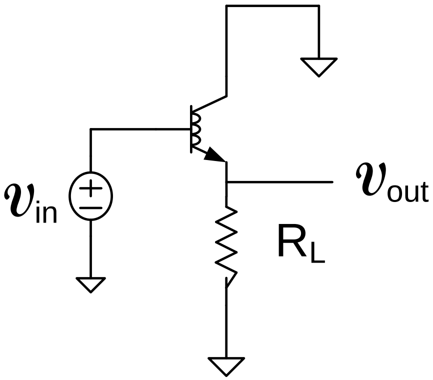
Biasing components shown in blue



Biased small-signal circuit

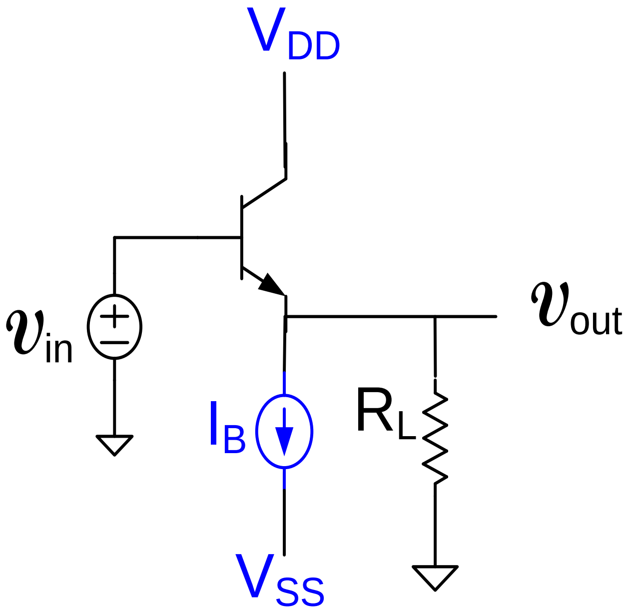
Amplifier Biasing

Example:



Desired small-signal circuit
Common Collector Amplifier

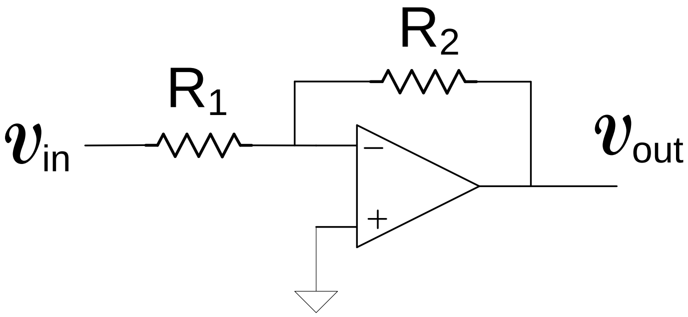
Biasing components shown in blue



Biased circuit

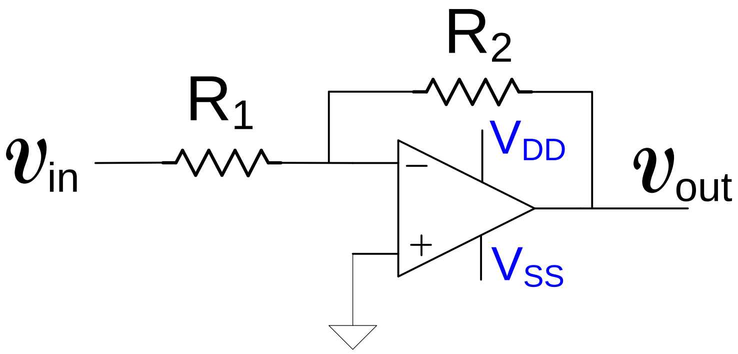
Amplifier Biasing

Example:



Desired small-signal circuit
Inverting Feedback Amplifier

Biasing components shown in blue



Biased circuit

Basic Amplifier Structures

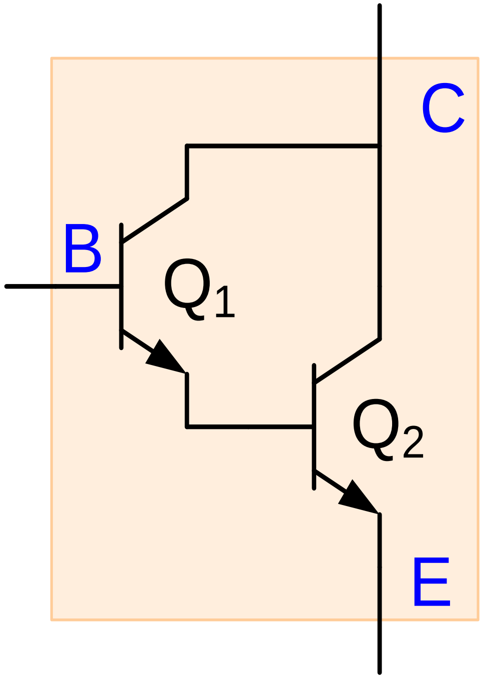
1. Common Emitter/Common Source
2. Common Collector/Common Drain
3. Common Base/Common Gate
4. Common Emitter with R_E/ Common Source with R_S

5. Cascode (actually CE:CB or CS:CG cascade)
6. Darlington (special CC:CC or CD:CD (approx) cascade)

Will be discussed later

The first 4 are most popular

Other Basic Configurations



Darlington Configuration

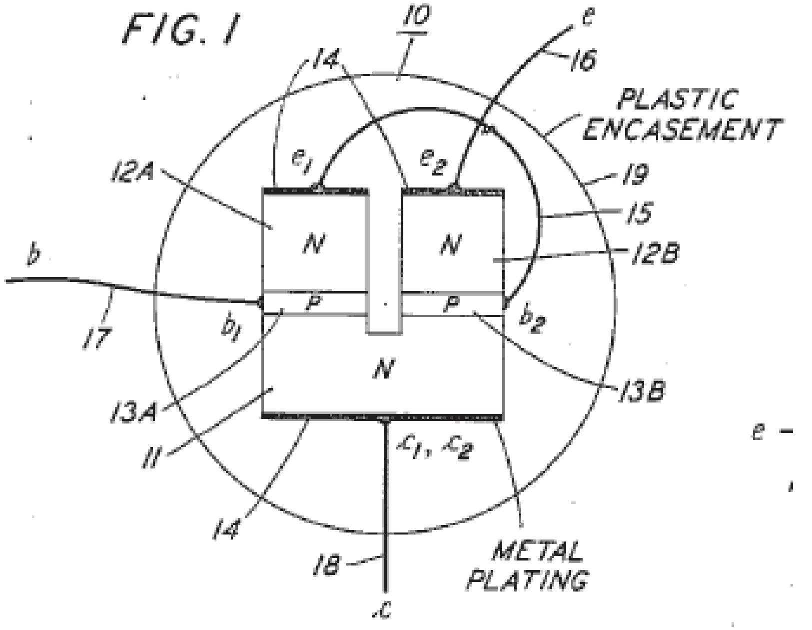


FIG. 1

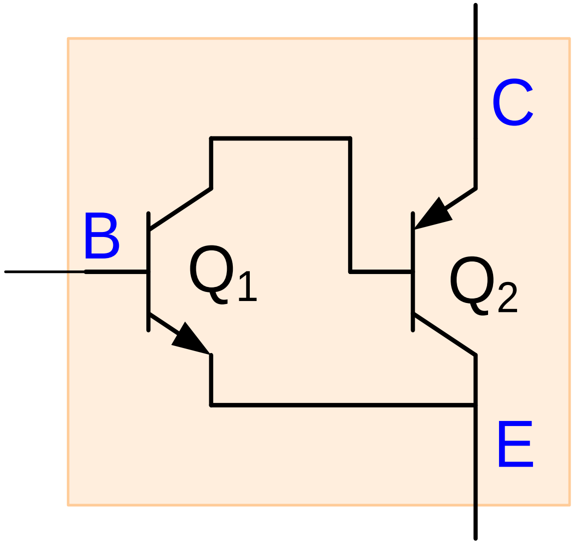
S. DARLINGTON 2,663,806

SEMICONDUCTOR SIGNAL TRANSLATING DEVICE

Filed May 9, 1952

- **Current gain is approximately β^2**
- **Two diode drop between B_{eff} and E_{eff}**

Other Basic Configurations



Sziklai Pair

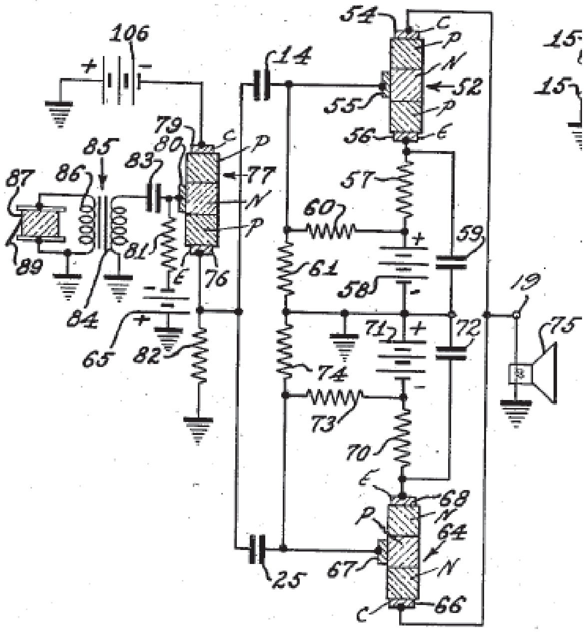


FIG. 3.

May 7, 1957 G. C. SZIKLAI 2,791,644

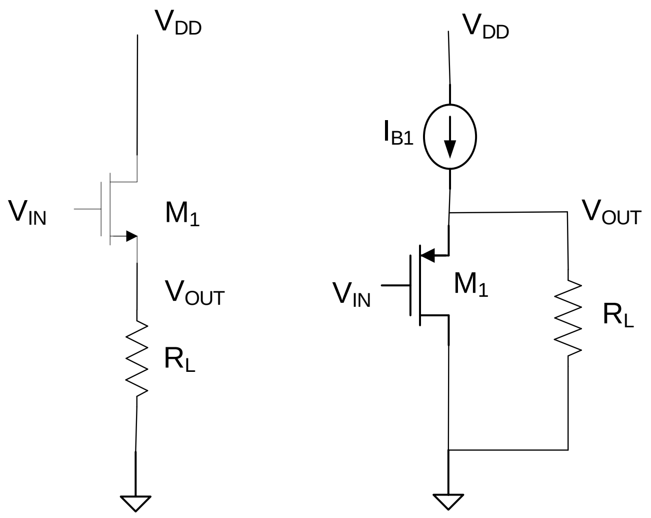
PUSH-PULL AMPLIFIER WITH COMPLEMENTARY TYPE TRANSISTORS

Filed Nov. 7, 1952

- Gain similar to that of Darlington Pair
- Current gain is approximately $\beta_n \beta_p$
- Current gain will not be as large when $\beta_p < \beta_n$
- Only one diode drop between B_{eff} and E_{eff}

Other Basic Configurations

Buffer



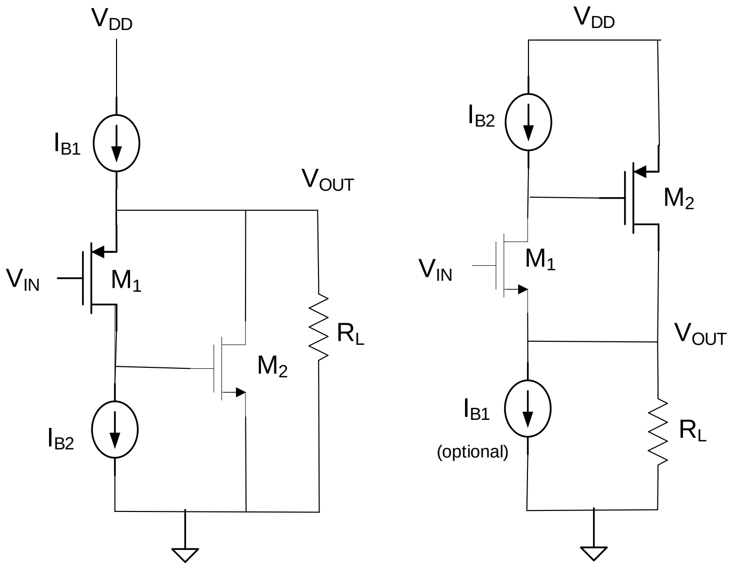
Ideally $V_{OUT}=V_{IN}$

Assume load terminated on gnd

Current through M_1 changes with V_{IN}

Voltage shift varies with V_{IN} in buffer

Super Buffer



Ideally $V_{OUT}=V_{IN}$

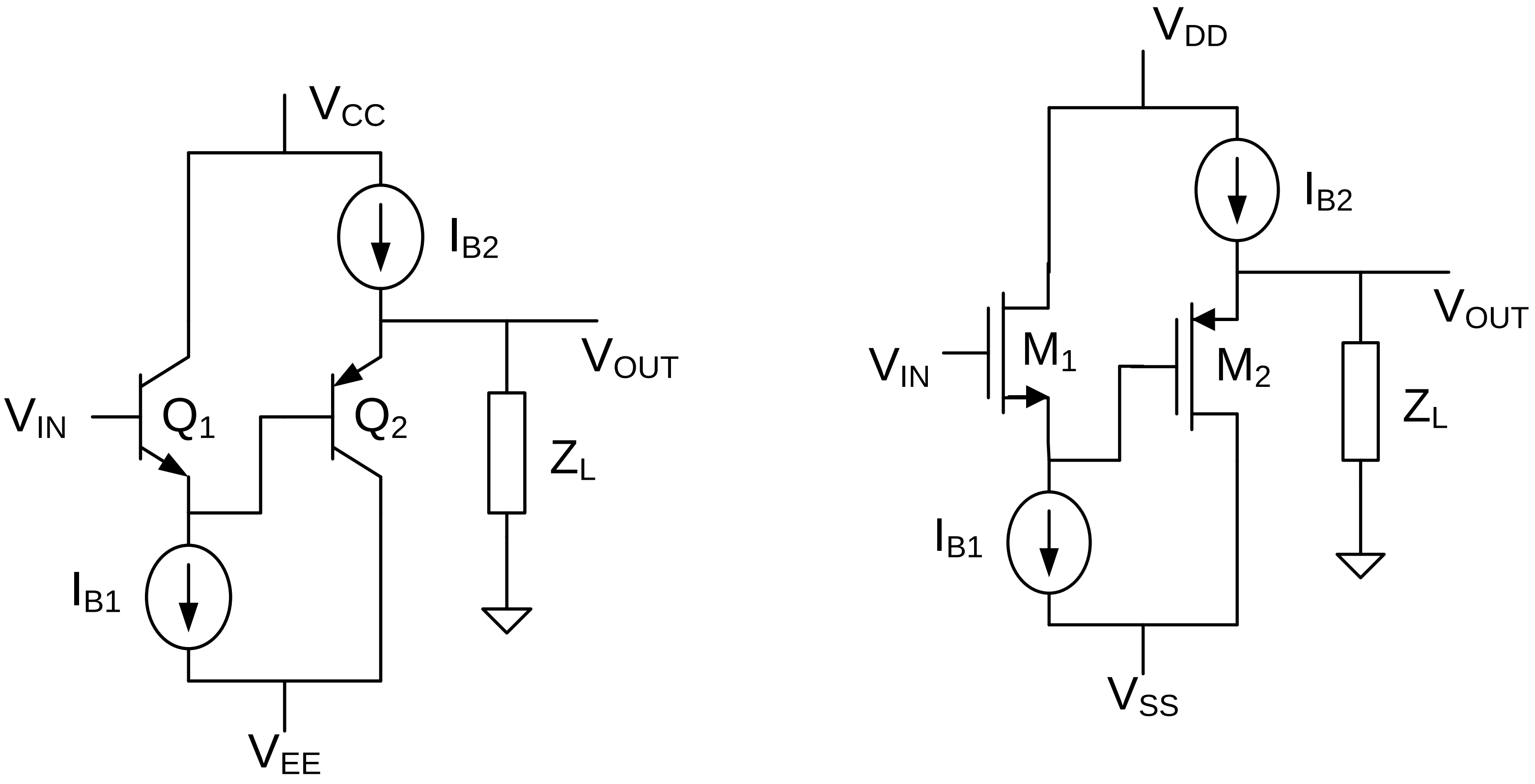
Assume load terminated on gnd

Current through shift transistor is constant for Super Buffer as V_{IN} changes so voltage shift does not change with V_{IN}

Same nominal voltage shift as buffer

Other Basic Configurations

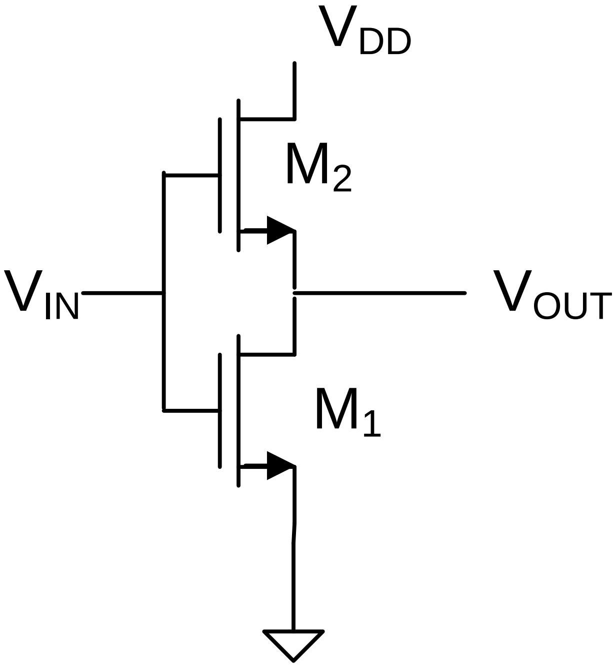
Low offset buffers

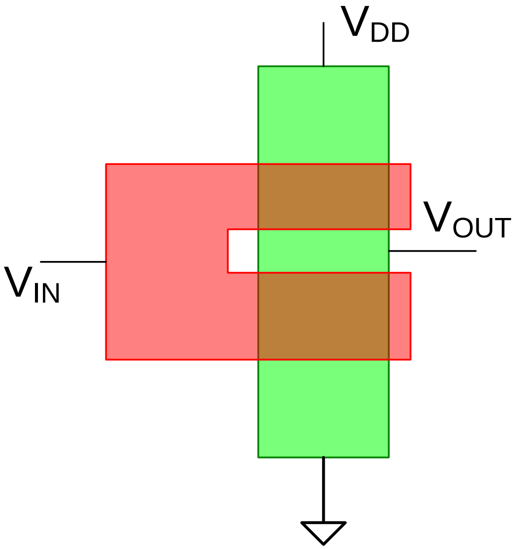


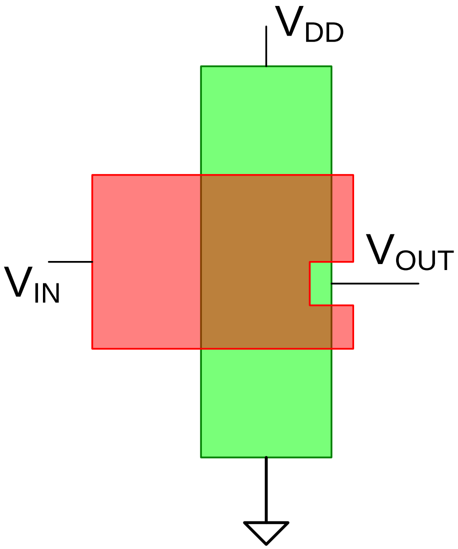
- **Actually a CC-CC or a CD-CD cascade**
- **Significant drop in offset between input and output**
- **Biasing with DC current sources**
- **Can Add Super Buffer to Output**

Other Basic Configurations

Voltage Attenuator

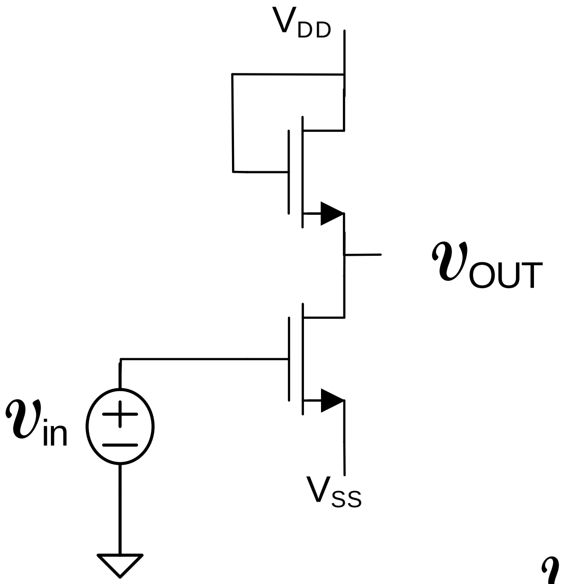




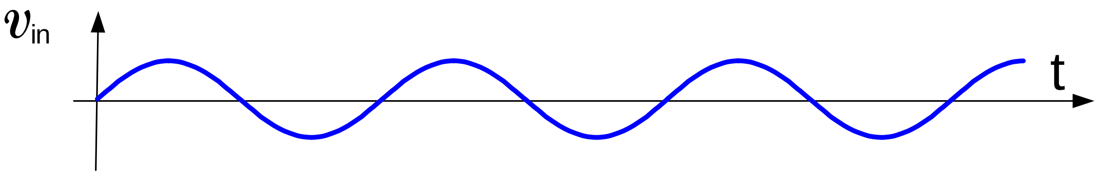


- **Attenuation factor is quite accurate (Determined by geometry)**
- **Infinite input impedance**
- **M_1 in triode, M_2 in saturation**
- **Actually can be a channel-tapped structure**

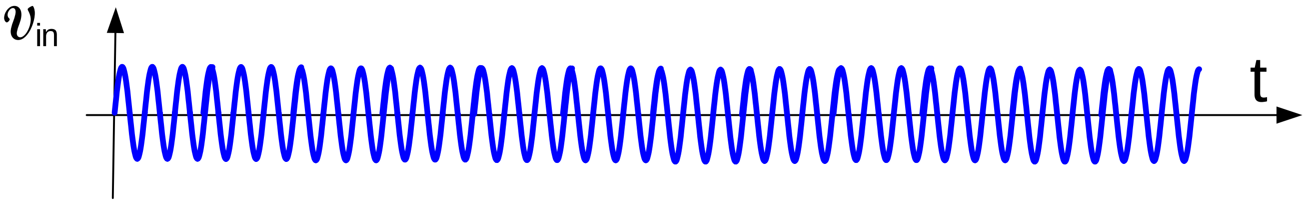
High Frequency Amplifier Performance



Up to this point it was assumed transistors can be modeled by their static I-V characteristics. This is justifiable if the frequency of the input is sufficiently low

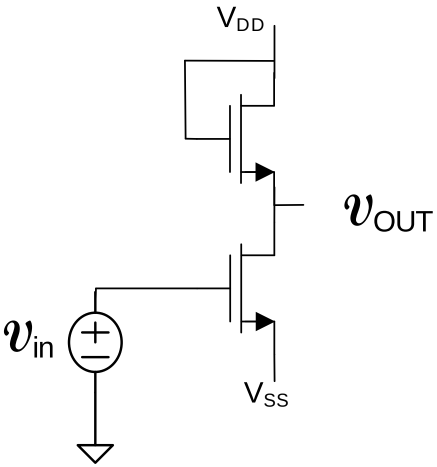


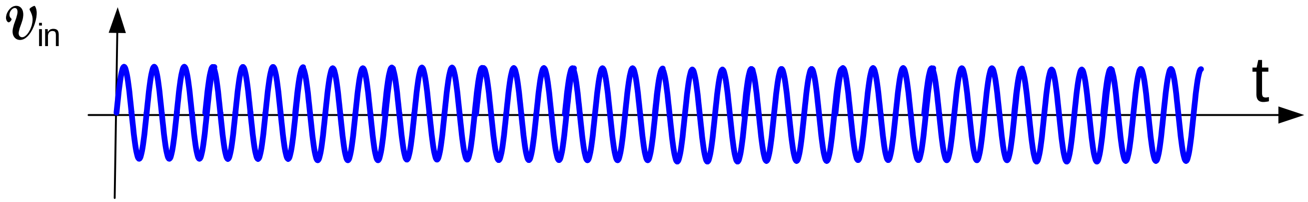
Consider now increasing the frequency of the input so this modeling assumption is no longer valid



As was observed earlier in the course with digital circuits, parasitic capacitors in the MOS transistors will limit the high frequency performance

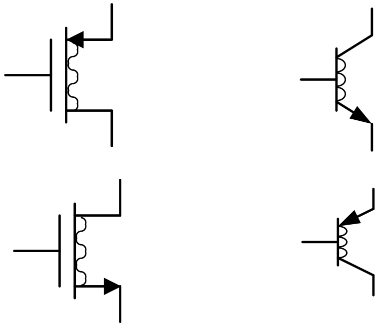
High Frequency Amplifier Performance





Parasitic capacitors in the MOS transistors will limit the high frequency performance

How can we predict performance of amplifiers (with small-signal inputs) at high frequencies?



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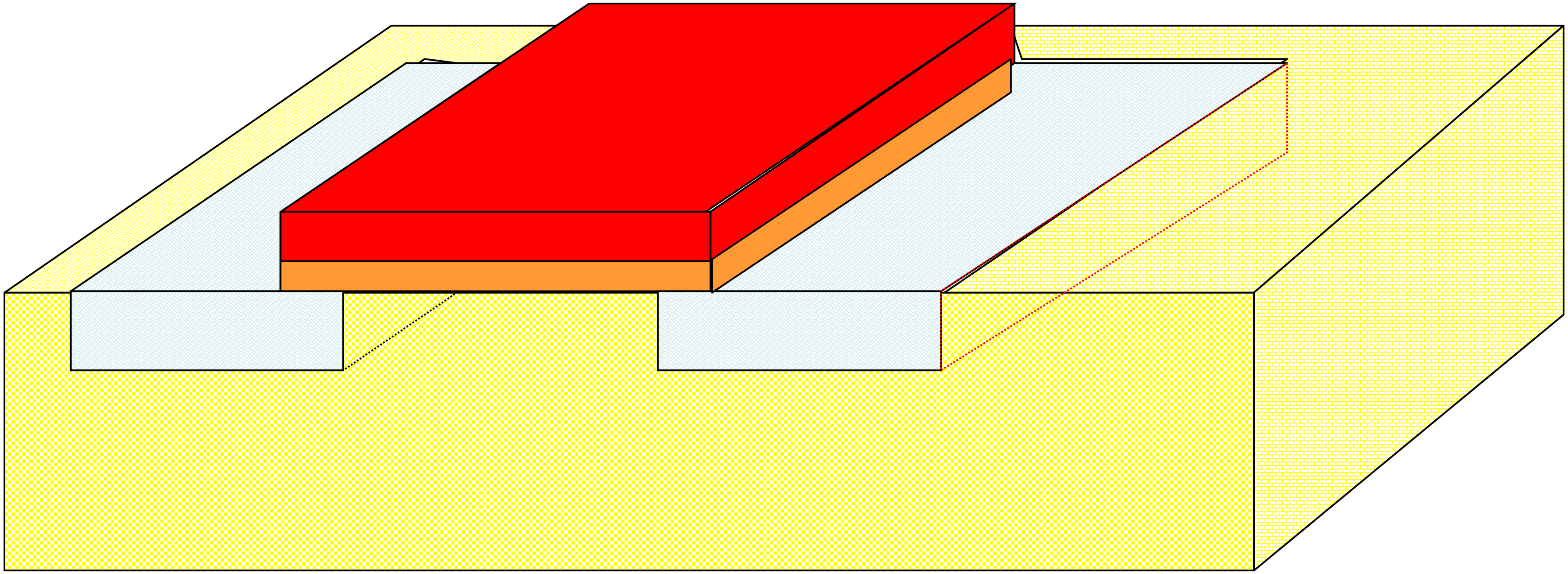
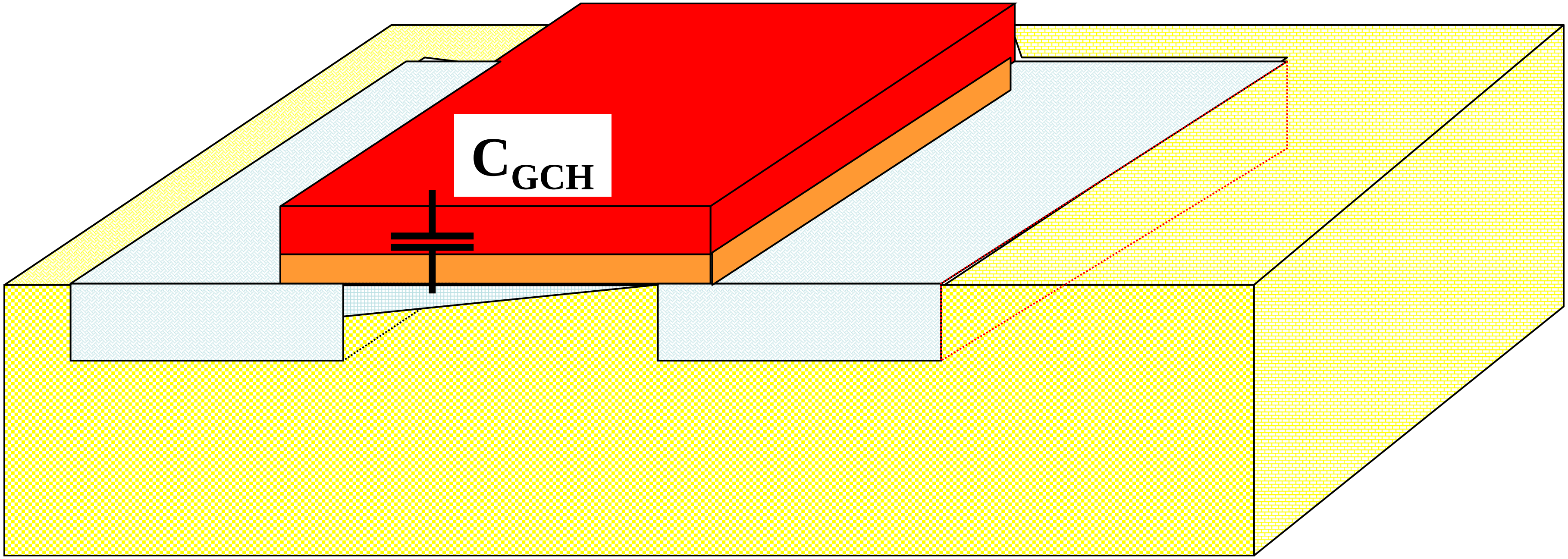
High Frequency
MOSFET Model

Parasitic Capacitors in MOSFET

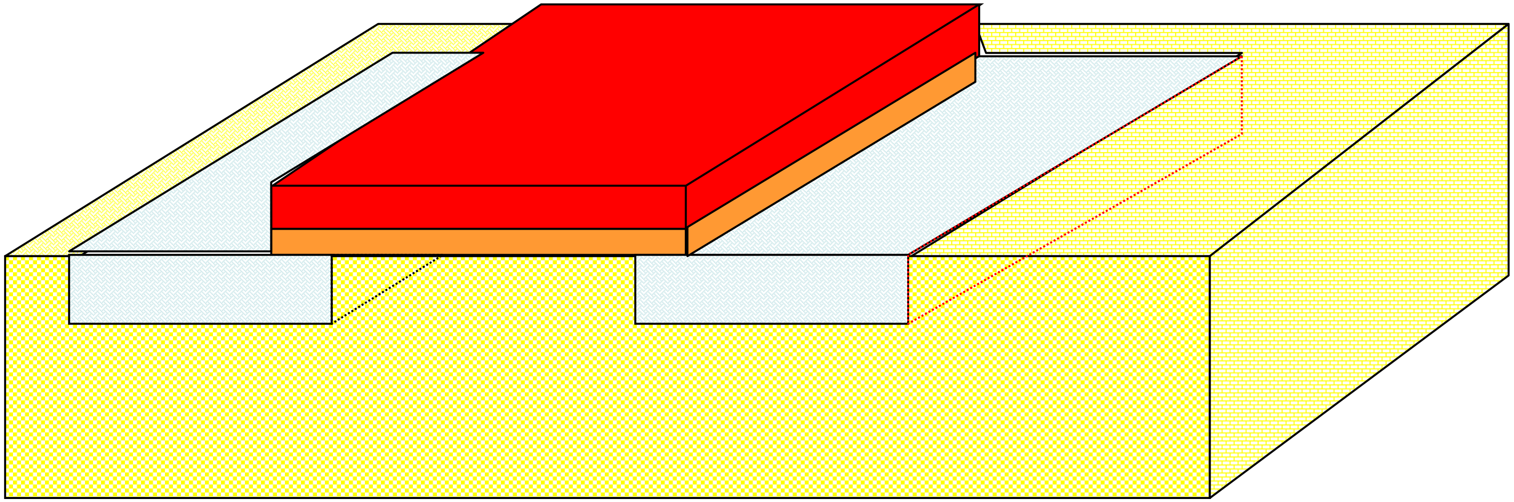


Parasitic Capacitors in MOSFET

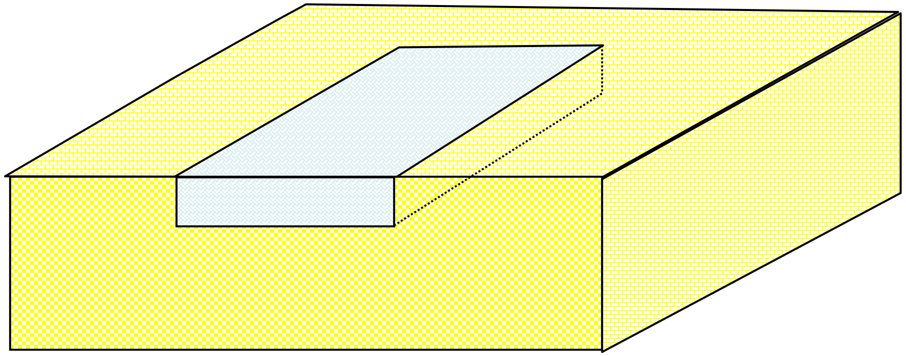


- This capacitance was modeled previously and exists when the transistor is operating in triode or saturation
- But there are others that also affect high-frequency or high-speed operation

Parasitic Capacitors in MOSFET

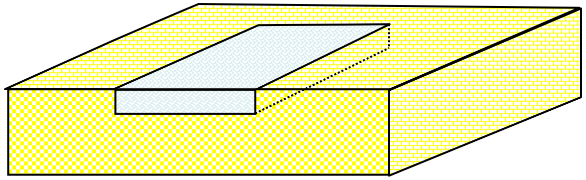


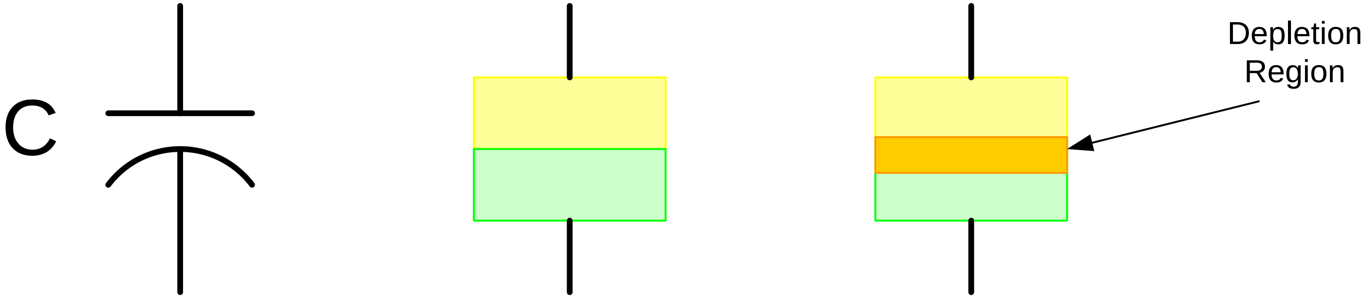
Recall that pn junctions have a depletion region!



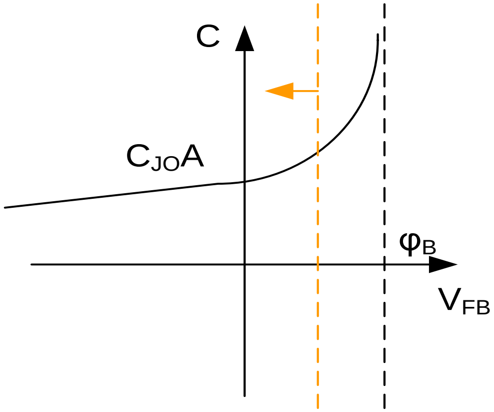
Parasitic Capacitors in MOSFET

pn junction capacitance





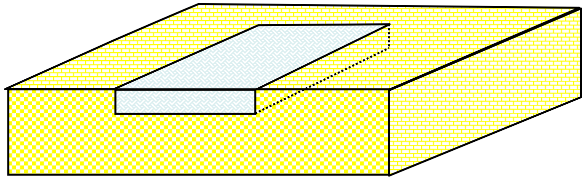
For $V_{FB}<\varphi_B/2$



$$C = \frac{C_{J0}A}{\left(1-\frac{V_{FB}}{\varphi_B}\right)^m}$$

Parasitic Capacitors in MOSFET

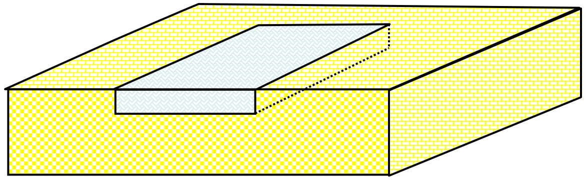
pn junction capacitance

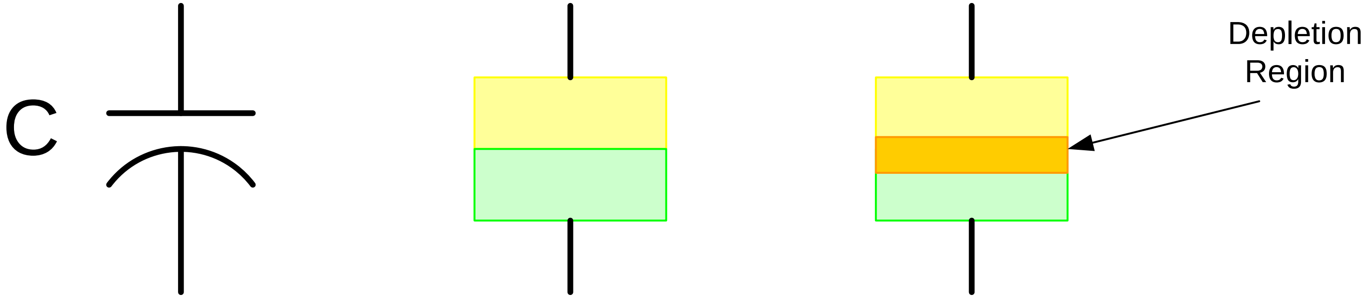


The bottom and the sidewall:

Parasitic Capacitors in MOSFET

pn junction capacitance





For a pn junction capacitor

$$C_J = C_{BOT}A + C_{SW}P$$

$$C_{BOT} = \frac{C_{BOT0}}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m} \qquad C_{SW} = \frac{C_{SW0}}{\left(1 - \frac{V_{FB}}{\varphi_B}\right)^m}$$

A : Junction Area

P: Junction Perimeter

V_{FB}: forward bias on junction

Model Parameters:

$\{C_{BOT0}, C_{SW0}, \varphi_B, m\}$

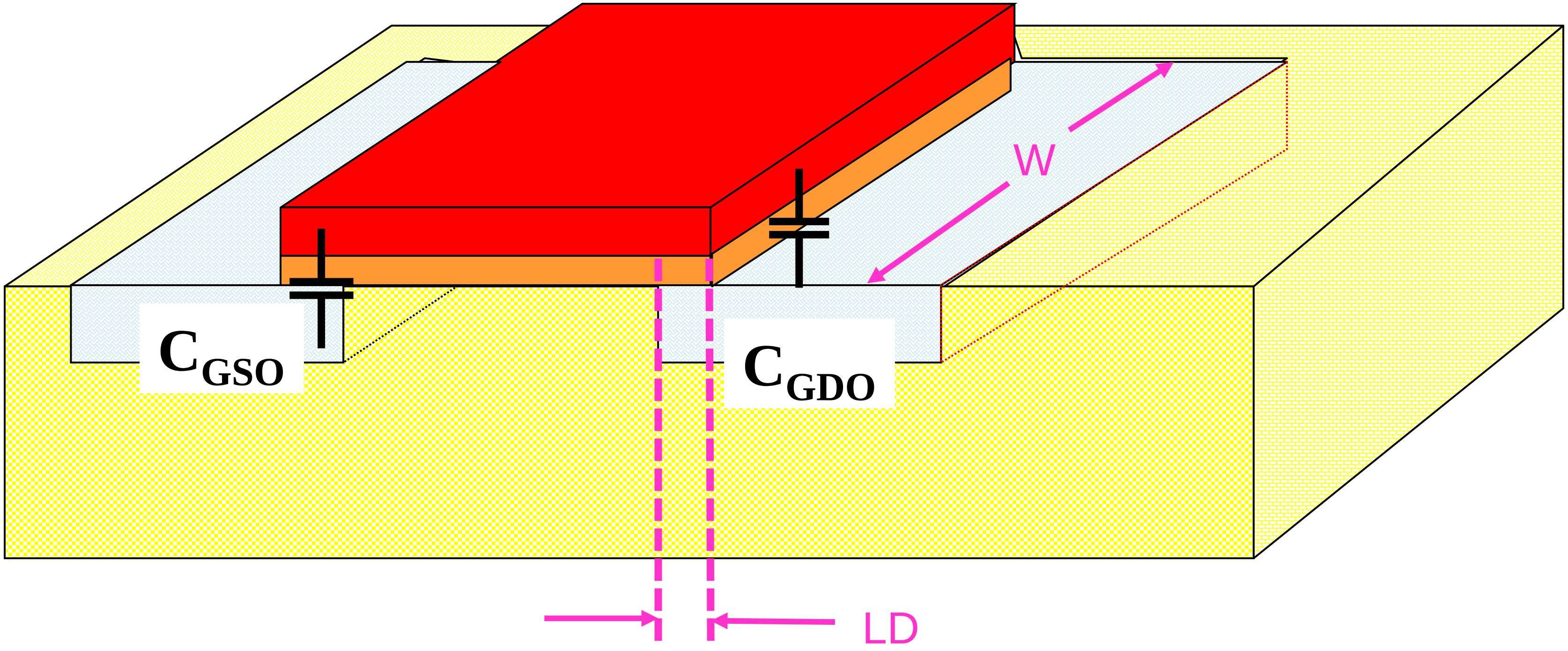
C_{BOT} and C_{SW} are capacitance densities

Types of Capacitors in MOSFETs

1. Fixed Capacitors
    1. Fixed Geometry
    2. Junction
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

Fixed Capacitors – Fixed Geometry

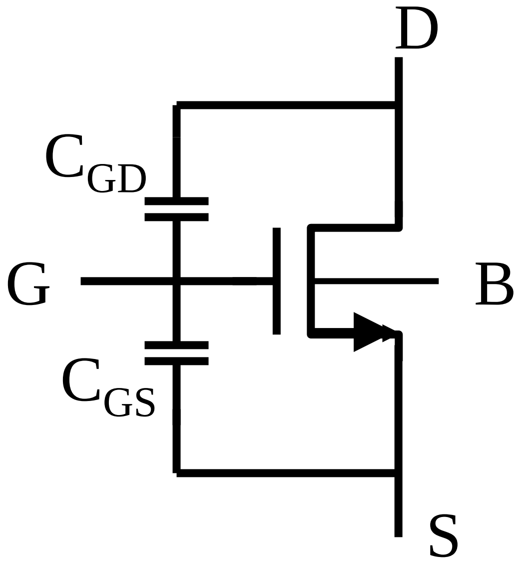


Overlap Capacitors: C_{GDO}, C_{GSO}

Cap Density: C_{OX}

L_D: lateral diffusion

Parasitic Capacitance Summary (partial)



	Cutoff	**Ohmic**	**Saturation**
C_{GSO}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$
C_{GDO}	$C_{ox}WL_D$	$C_{ox}WL_D$	$C_{ox}WL_D$

L_D is a model parameter

Overlap Capacitance Model Parameters

```
CAPACITANCE PARAMETERS N+ P+ POLY  M1 M2 M3 M4 M5 M6 R_W  D_N_W M5P N_W  UNITS
 Area (substrate)     942 1163 106 34 14  9  6  5  3         123    125 aF/um^2
 Area (N+active)              8484 55 20 13 11  9  8                    aF/um^2
 Area (P+active)              8232                                      aF/um^2
 Area (poly)                       66 17 10  7  5  4                    aF/um^2
 Area (metal1)                        37 14  9  6  5                    aF/um^2
 Area (metal2)                           35 14  9  6                    aF/um^2
 Area (metal3)                              37 14  9                    aF/um^2
 Area (metal4)                                 36 14                    aF/um^2
 Area (metal5)                                    34              984   aF/um^2
 Area (r well)         920                                              aF/um^2
 Area (d well)                                          582             aF/um^2
 Area (no well)        137                                              aF/um^2
 Fringe (substrate)    212  235    41 35 29 21 14                        aF/um
 Fringe (poly)                     70 39 29 23 20 17                     aF/um
 Fringe (metal1)                      52 34    22 19                     aF/um
 Fringe (metal2)                         48 35 27 22                     aF/um
 Fringe (metal3)                            53 34 27                     aF/um
 Fringe (metal4)                               58 35                     aF/um
 Fringe (metal5)                                  55                     aF/um
 Overlap (N+active)             895                                      aF/um
 Overlap (P+active)             737                                      aF/um
```

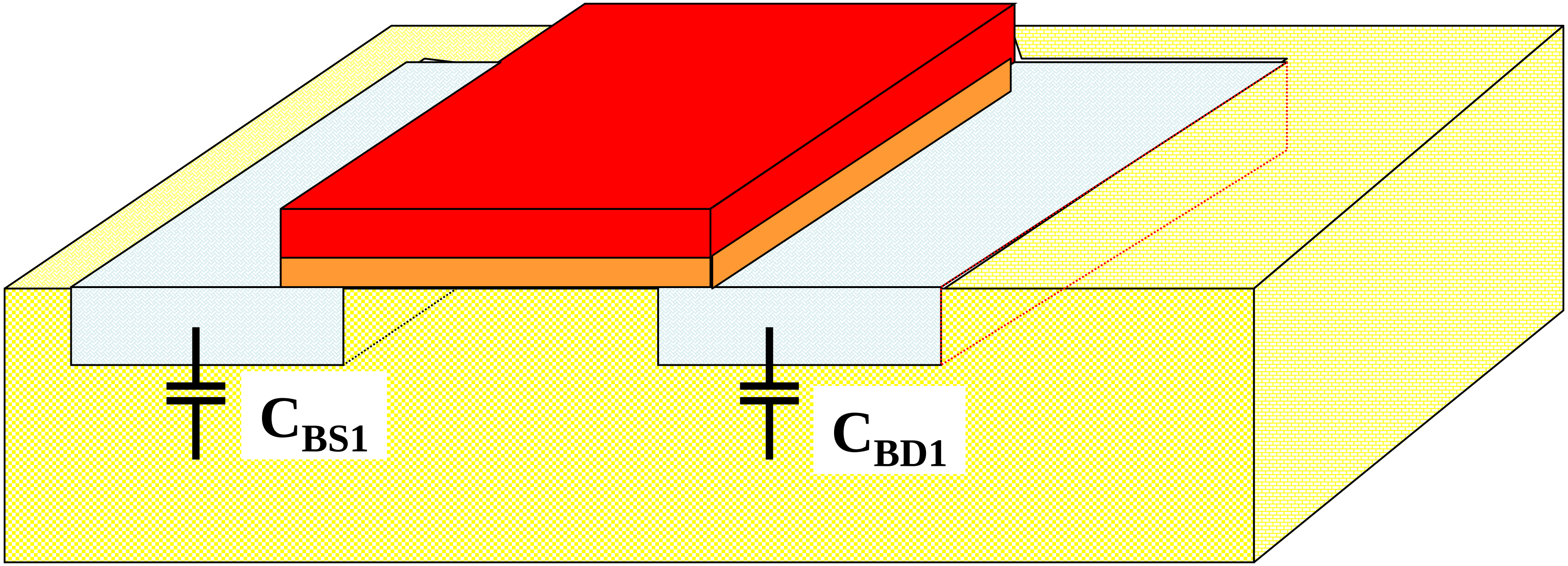
Types of Capacitors in MOSFETs

1. Fixed Capacitors
    a. Fixed Geometry
    b. Junction

2. Operating Region Dependent

Parasitic Capacitors in MOSFET

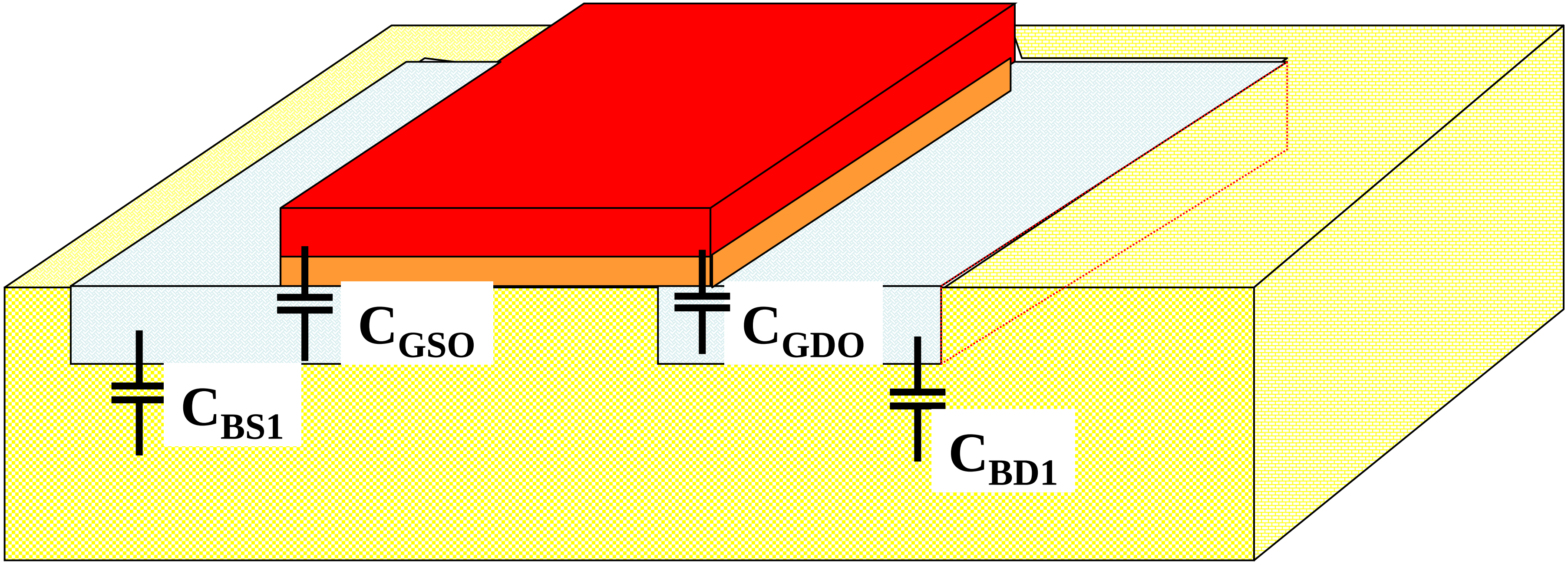
Fixed Capacitors- Junction



Junction Capacitors: C_{BS1}, C_{BD1}

Parasitic Capacitors in MOSFET

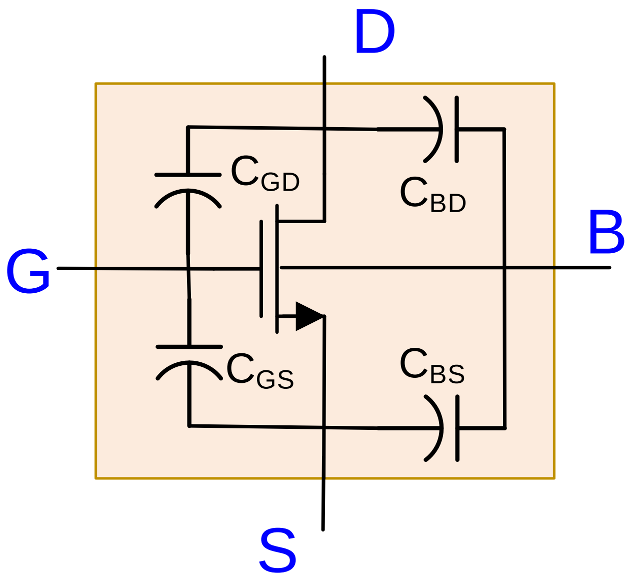
- Fixed Capacitors



Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Fixed Parasitic Capacitance Summary



C_{BOT} and C_{SW} are model parameters

	Cutoff	**Ohmic**	**Saturation**
C_{GSO}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{GDO}	$CoxWL_D$	$CoxWL_D$	$CoxWL_D$
C_{BG}			
C_{BS}	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$	$C_{BS1} = C_{BOT}A_S+C_{SW}P_S$
C_{BD}	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$	$C_{BD1} = C_{BOT}A_D+C_{SW}P_D$

C_{BOT} and C_{SW} model parameters

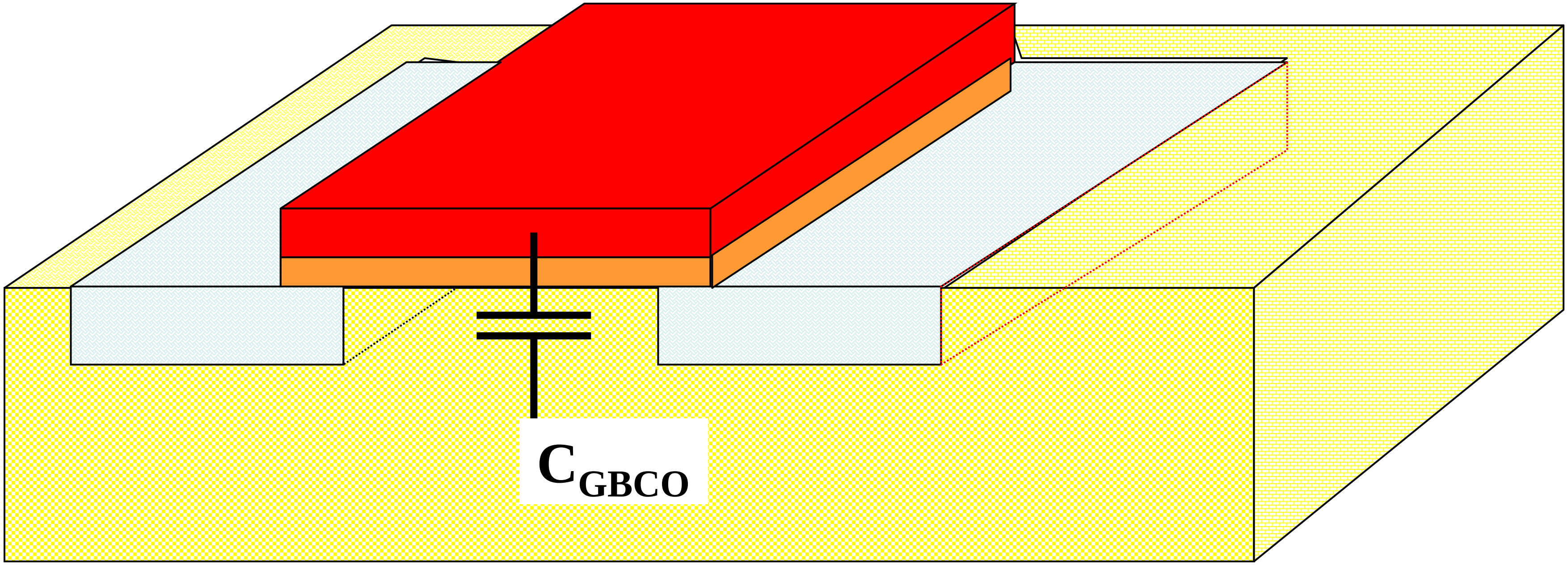
```
CAPACITANCE PARAMETERS N+ P+ POLY  M1 M2 M3 M4 M5 M6 R_W  D_N_W M5P N_W  UNITS
 Area (substrate)     942 1163 106 34 14  9  6  5  3         123    125 aF/um^2
 Area (N+active)              8484 55 20 13 11  9  8                    aF/um^2
 Area (P+active)              8232                                      aF/um^2
 Area (poly)                       66 17 10  7  5  4                    aF/um^2
 Area (metal1)                        37 14  9  6  5                    aF/um^2
 Area (metal2)                           35 14  9  6                    aF/um^2
 Area (metal3)                              37 14  9                    aF/um^2
 Area (metal4)                                 36 14                    aF/um^2
 Area (metal5)                                    34              984   aF/um^2
 Area (r well)         920                                              aF/um^2
 Area (d well)                                          582             aF/um^2
 Area (no well)        137                                              aF/um^2
 Fringe (substrate)    212  235    41 35 29 21 14                        aF/um
 Fringe (poly)                     70 39 29 23 20 17                     aF/um
 Fringe (metal1)                      52 34    22 19                     aF/um
 Fringe (metal2)                         48 35 27 22                     aF/um
 Fringe (metal3)                            53 34 27                     aF/um
 Fringe (metal4)                               58 35                     aF/um
 Fringe (metal5)                                  55                     aF/um
 Overlap (N+active)             895                                      aF/um
 Overlap (P+active)             737                                      aF/um
```

Types of Capacitors in MOSFETs

1. Fixed Capacitors
    a. Fixed Geometry
    b. Junction
2. Operating Region Dependent

Parasitic Capacitors in MOSFET

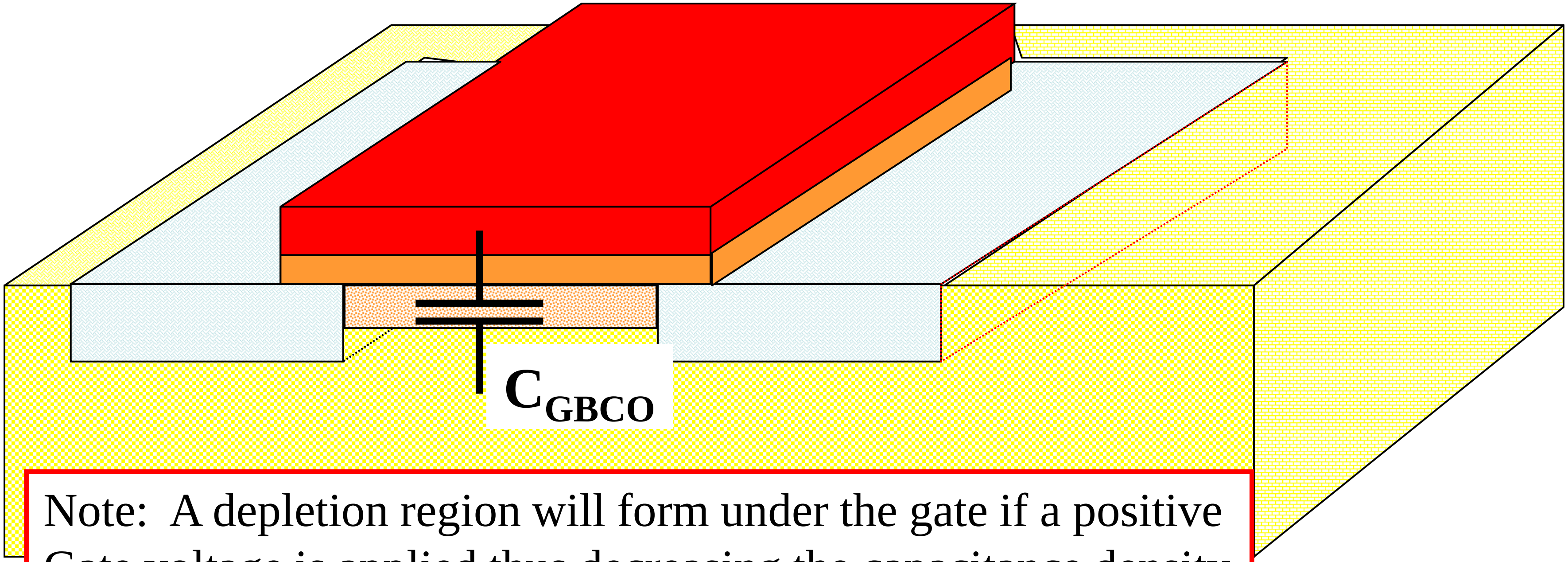
Operation Region Dependent -- Cutoff



Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Cutoff

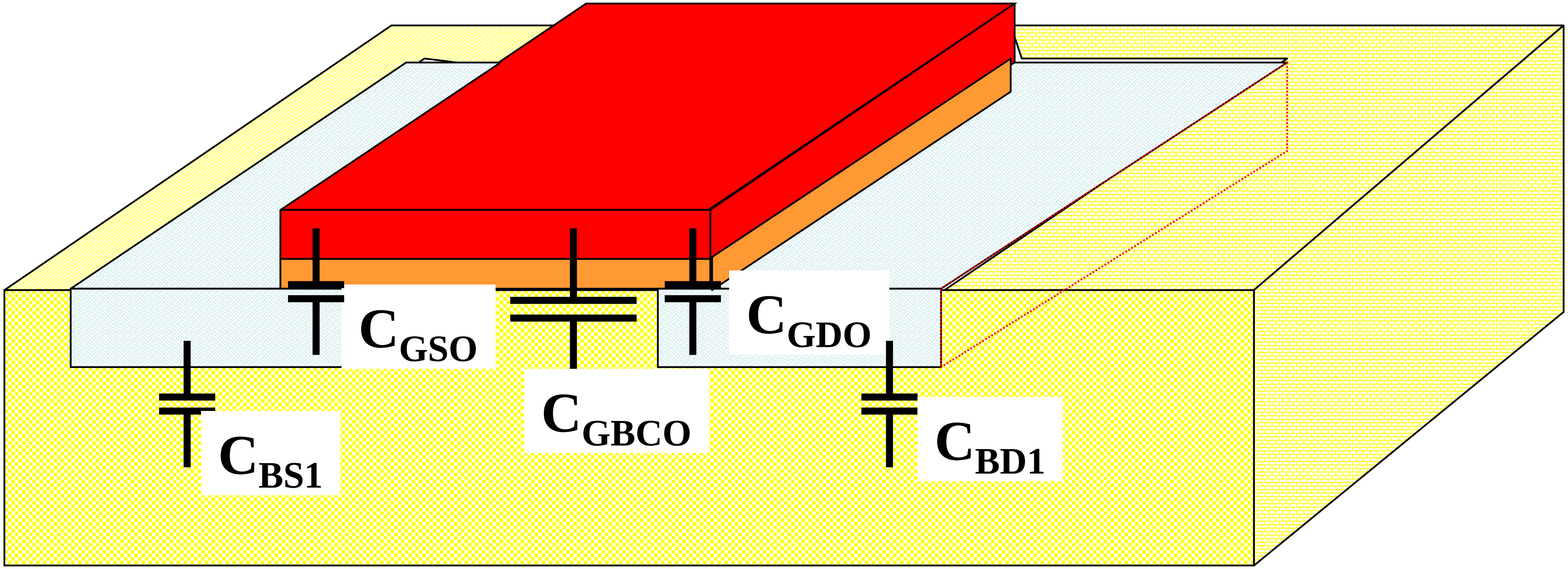


Note: A depletion region will form under the gate if a positive Gate voltage is applied thus decreasing the capacitance density

Cutoff Capacitor: C_{GBCO}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Cutoff

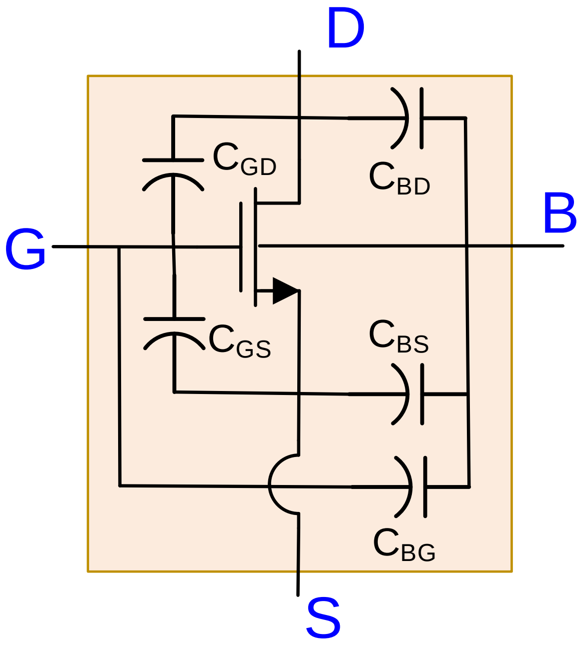


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Cutoff Capacitor: C_{GBCO}

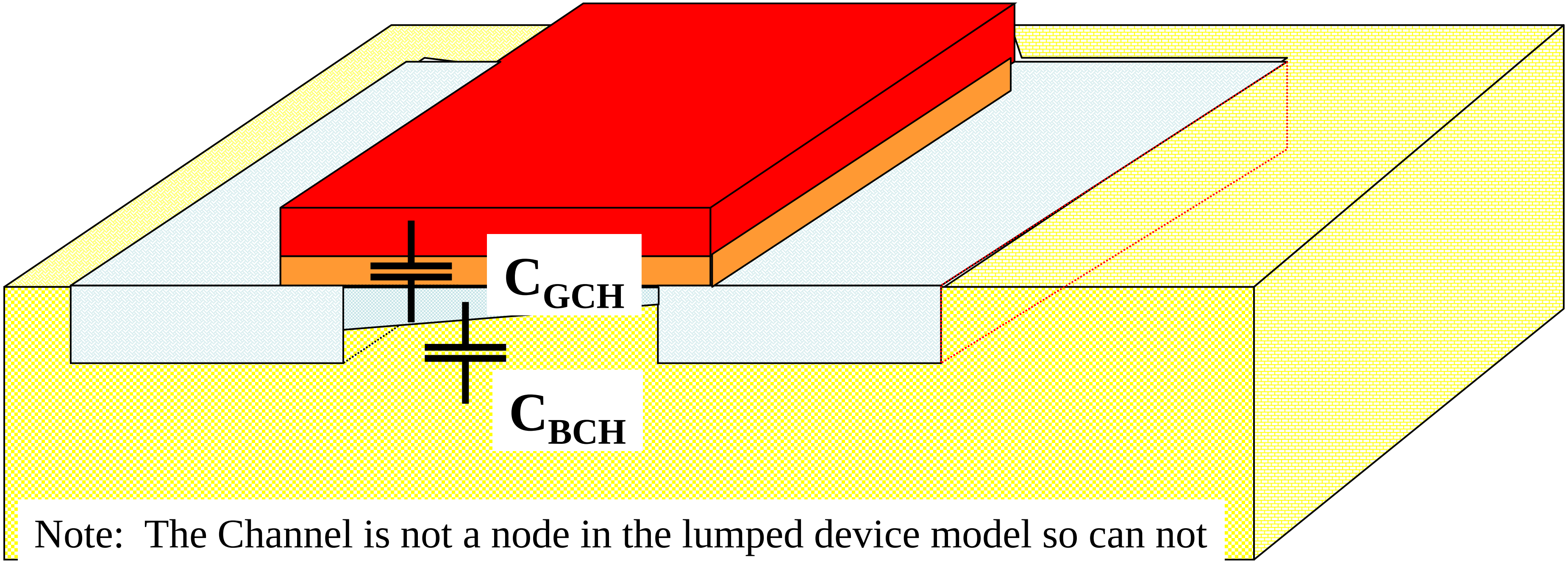
Parasitic Capacitance Summary



	Cutoff	**Ohmic**	**Saturation**
C_{GSO}	$C_{ox}WL_D$		
C_{GDO}	$C_{ox}WL_D$		
C_{BG}	$C_{ox}WL$ (or less)		
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$		
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$		

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Ohmic



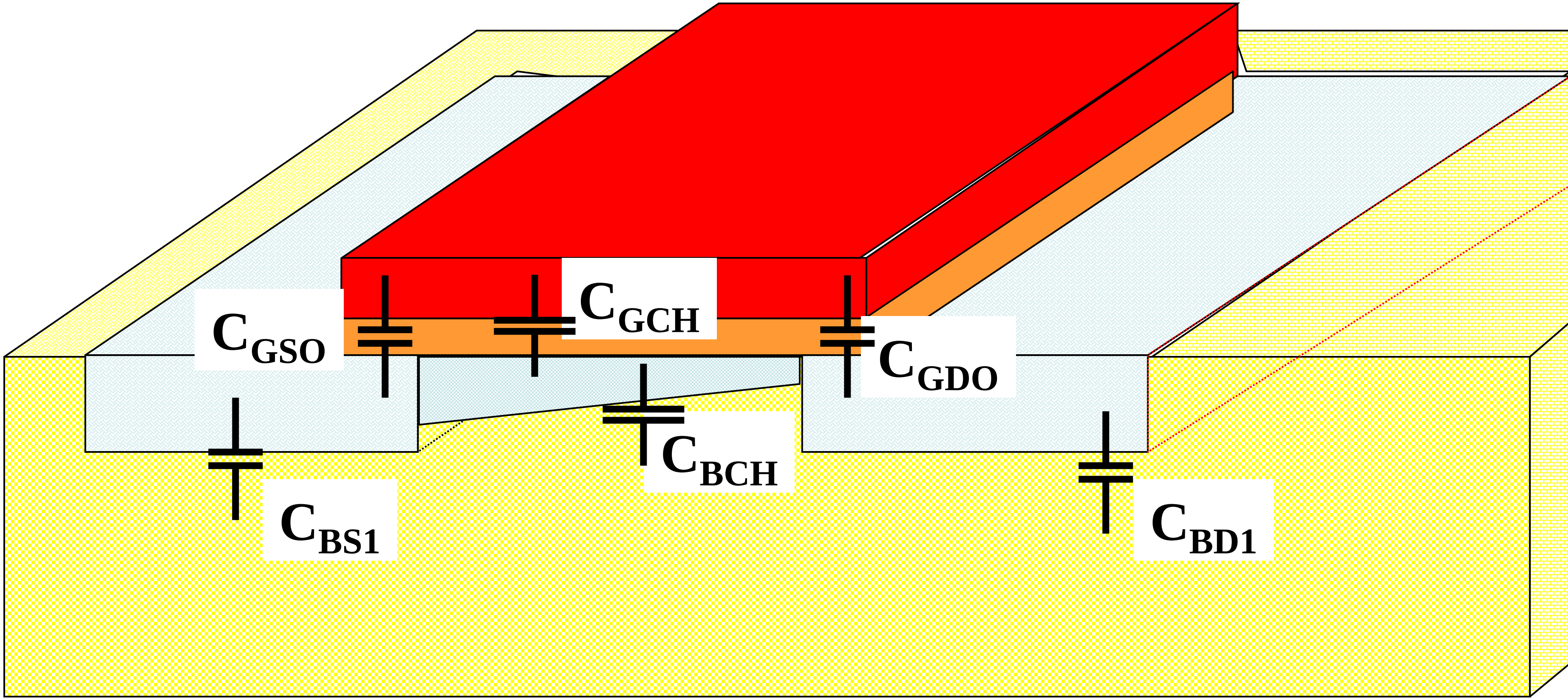
Note: The Channel is not a node in the lumped device model so can not directly include this distributed capacitance in existing models

Note: The distributed channel capacitance is usually lumped and split evenly between the source and drain nodes

Ohmic Capacitor: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed -- Ohmic

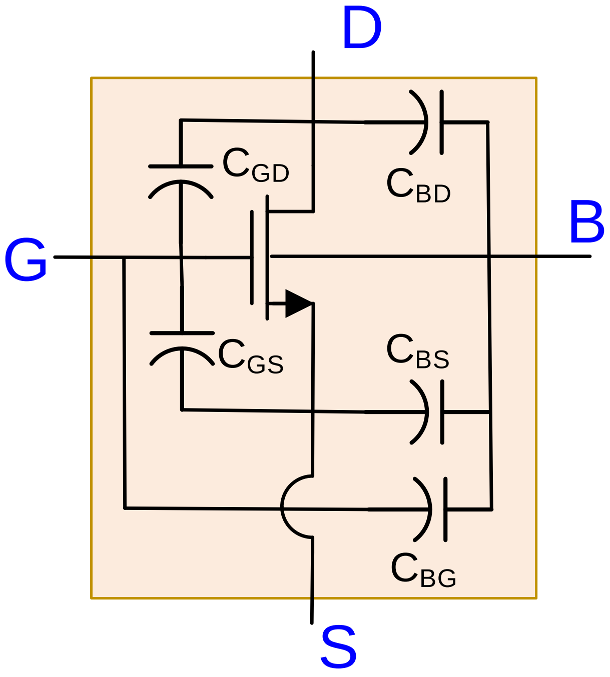


Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Ohmic Capacitor: C_{GCH} , C_{BCH}

Parasitic Capacitance Summary

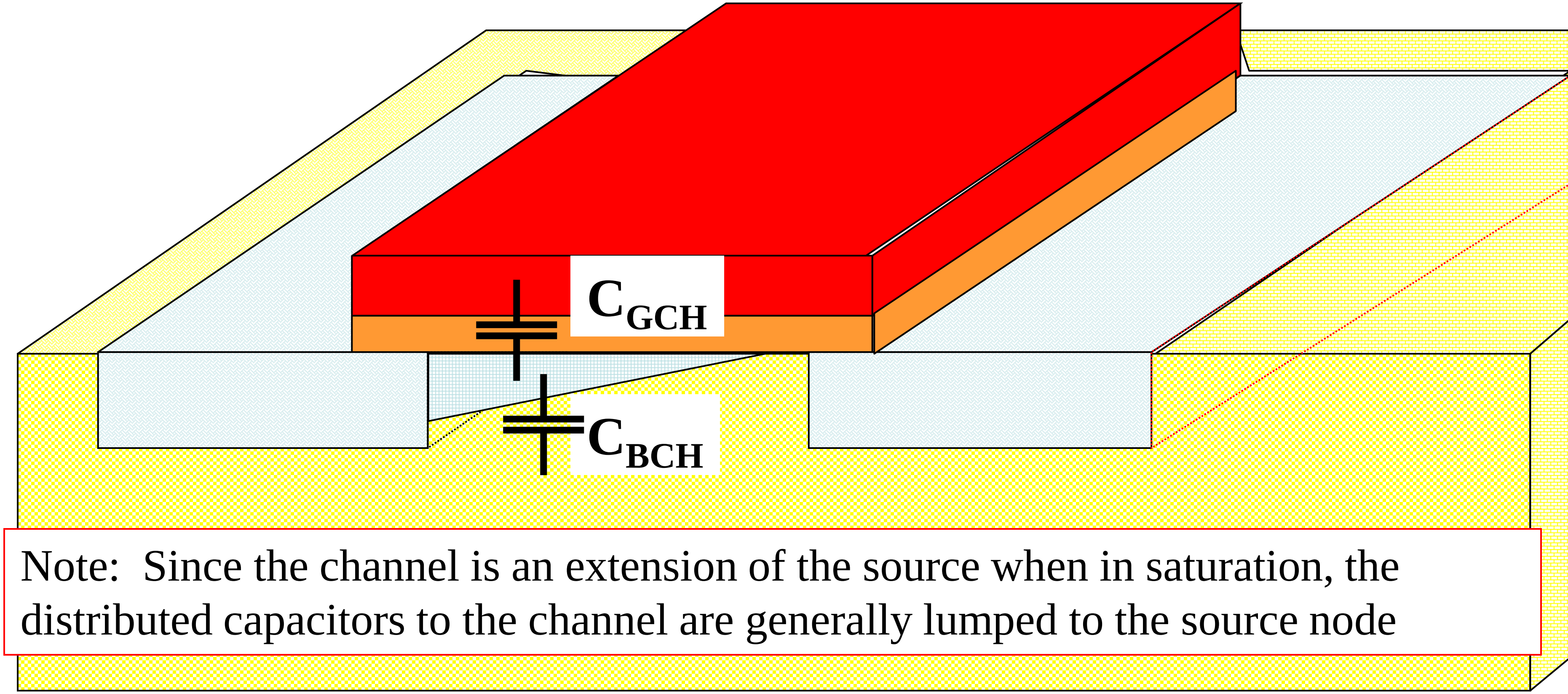


Lumped C_{GC} and C_{BC} to analytically avoid dealing with distributed capacitance

	Cutoff	**Ohmic**	**Saturation**
C_{GS}	$C_{ox}WL_D$	$0.5C_{ox}WL$	
C_{GD}	$C_{ox}WL_D$	$0.5C_{ox}WL$	
C_{BG}	$C_{ox}WL$ (or less)	0	
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	

Parasitic Capacitors in MOSFET

Operation Region Dependent -- Saturation

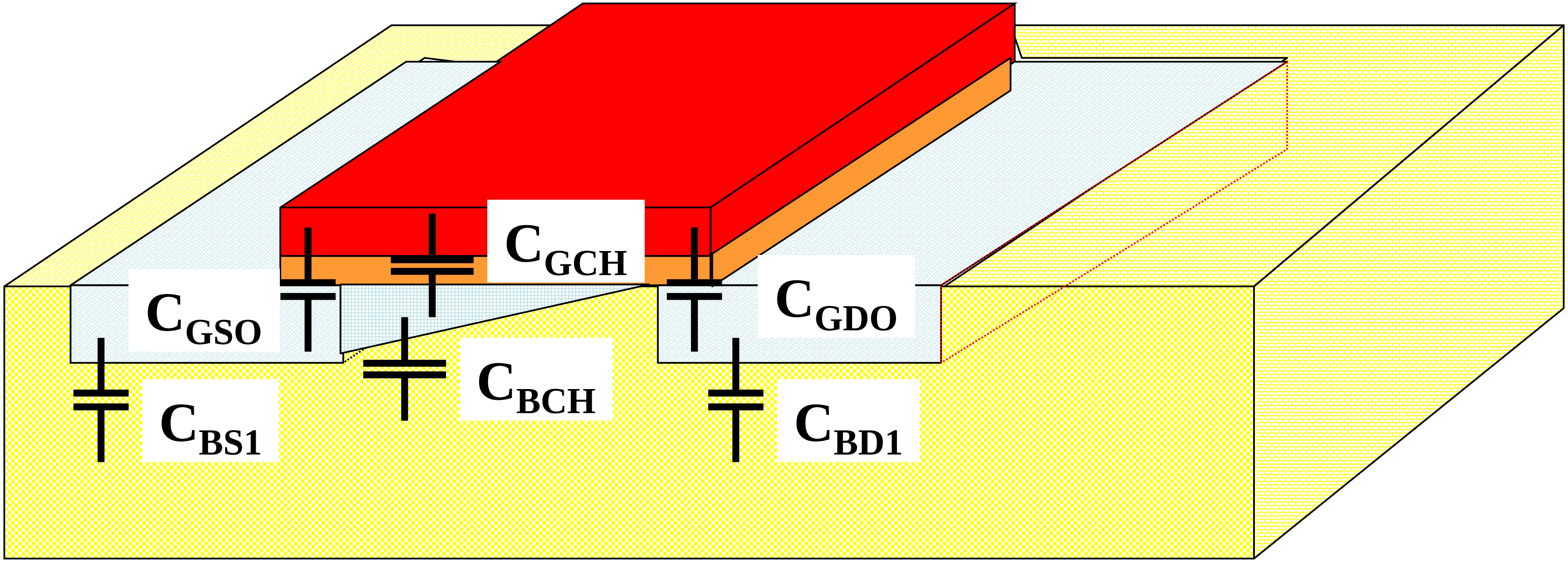


Note: Since the channel is an extension of the source when in saturation, the distributed capacitors to the channel are generally lumped to the source node

Saturation Capacitors: C_{GCH} , C_{BCH}

Parasitic Capacitors in MOSFET

Operation Region Dependent and Fixed --Saturation



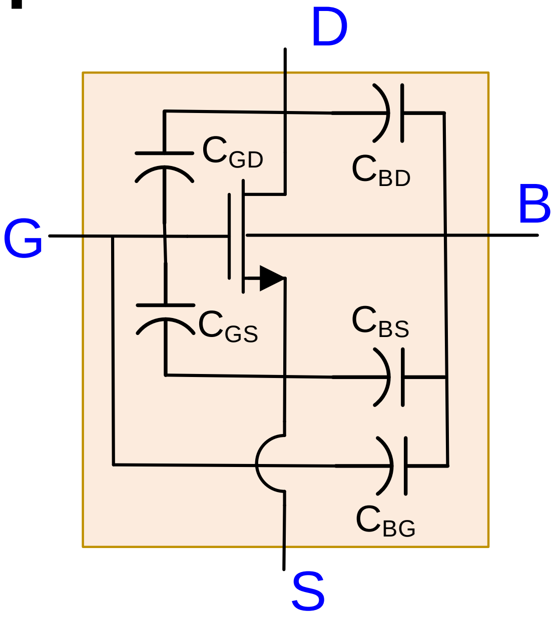
Overlap Capacitors: C_{GDO}, C_{GSO}

Junction Capacitors: C_{BS1}, C_{BD1}

Saturation Capacitors: C_{GCH} , C_{BCH}

- 2/3 $C_{OX}WL$ is often attributed to C_{GCH} to account for LD and saturation
- This approximation is reasonable for minimum-length devices but not so good for longer devices

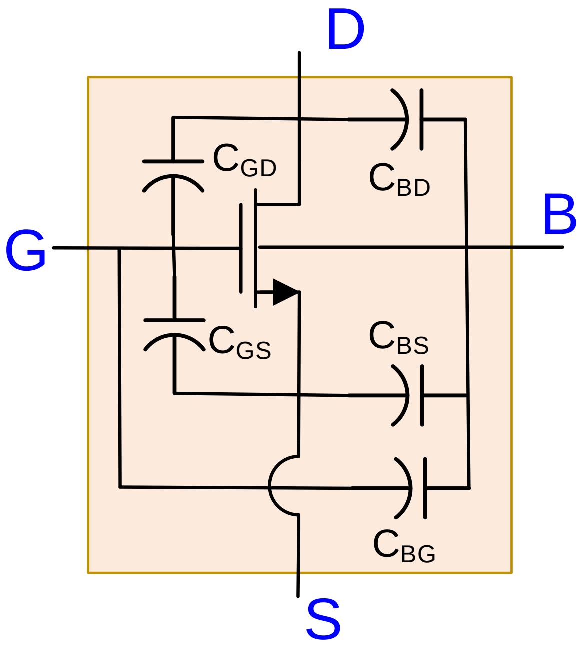
Parasitic Capacitance Summary



Lumped C_{GC} and C_{BC} to analytically avoid dealing with distributed capacitance

	Cutoff	**Ohmic**	**Saturation**
C_{GS}	$C_{ox}WL_D$	$0.5C_{OX}WL$	$C_{ox}WL_D+(2/3)C_{OX}WL$
C_{GD}	$C_{ox}WL_D$	$0.5C_{OX}WL$	$C_{ox}WL_D$
C_{BG}	$C_{ox}WL$ (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

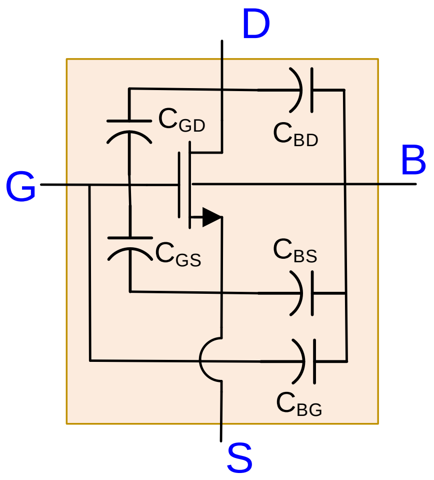
Parasitic Capacitance Summary



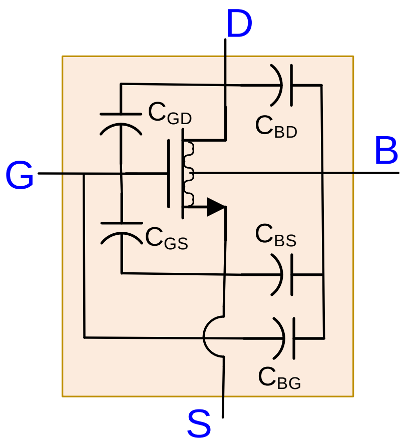
	Cutoff	Ohmic	Saturation
C_{GS}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D+(2/3)C_{OX}WL$
C_{GD}	$CoxWL_D$	$0.5C_{OX}WL$	$CoxWL_D$
C_{BG}	CoxWL (or less)	0	0
C_{BS}	$C_{BOT}A_S+C_{SW}P_S$	$C_{BOT}A_S+C_{SW}P_S+0.5WLC_{BOTCH}$	$C_{BOT}A_S+C_{SW}P_S+(2/3)WLC_{BOTCH}$
C_{BD}	$C_{BOT}A_D+C_{SW}P_D$	$C_{BOT}A_D+C_{SW}P_D+0.5WLC_{BOTCH}$	$C_{BOT}A_D+C_{SW}P_D$

Observe there is no C_{DS} in this model because does not physically exist

Parasitic Capacitance Summary

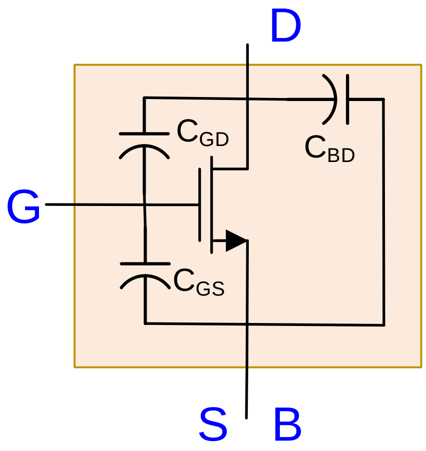


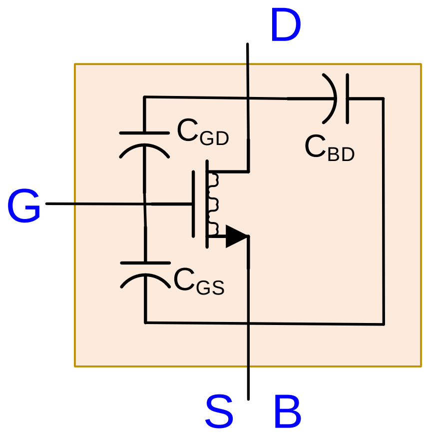
High Frequency Large Signal Model



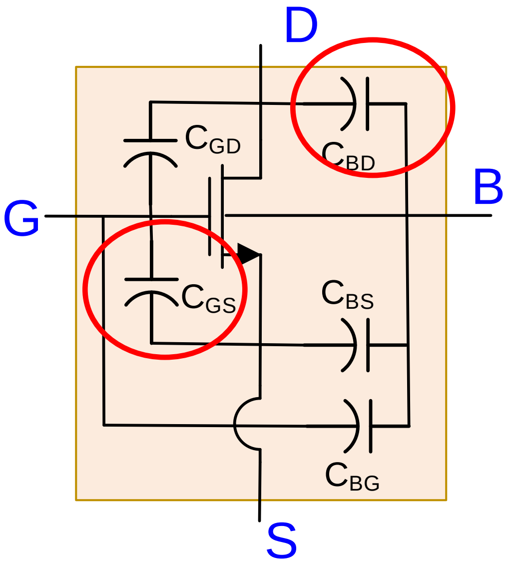
High Frequency Small Signal Model

Often V_{BS}=0 and C_{BG}=0, so simplifies to





Parasitic Capacitance Implications



The parasitic capacitances inherently introduce an upper limit on how fast either digital circuits or analog circuits can operate in a given process

Two parameters, f_{MAX} and f_T, (not defined yet) are two metric that are used to specify the fundamental speed limit in a semiconductor process

The dominant parasitic capacitances for most circuits are C_{GS} and C_{BD}

Stay Safe and Stay Healthy !

End of Lecture 35